31st International

Electronics Manufacturing Technology Symposium (IEMT 2006)

8-10 November 2006 Petaling Jaya, Kuala Lumpur, MALAYSIA

The 31st IEMT is an international event organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from the CPMT Society of IEEE and the Santa Clara Valley CPMT Chapter, featuring short courses, 3 parallel tracks of technical sessions, and exhibitions. It provides good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation.

Professional Development Courses:

● Emerging Technology In IC Packaging ● Thermal Test Methods for Integrated Circuits ● Wafer Dicing Technology ● Design, Materials, Process and Reliability of Pb-Free Packaging and Assembly

Tabletop Exhibits space still available!
Contact Mr. Eric Ng, eric.ng@st.com

Keynote Speakers and Instructors

● Dr Rolf Aschenbrenner ● Dr Carlo Cognetti ● Dr Annette Teng Cheung ● Bernie Siegal ● Charles Vath ● Kin Gan ● Dr John Lau ● Yee Eh Horng ● Dr. Dongkai Shangguan

IEEE Member fee: RM720 (approx US$200)
Early Registration Rate through October 9

Visit our website for more information:

www.ieee.org.my/iemt2006

IEEE

CALL FOR PAPERS

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Technical Conference, Short Courses and Exhibition

International Electronics & Manufacturing Technology (IEMT 2007)

November 2007, San Jose, California, USA

I. Introduction

The International Electronics Manufacturing Technology (IEMT) Conference is the premier Technical Conference devoted to the manufacture (mainly the assembly/packaging aspects) of electronic, opto-electronic and MEMS devices and systems. IEMT is an established International Conference of long standing organized by the Components Packaging and Manufacturing Technology (CPMT) Society of IEEE. IEMT 2007 is being co-organized by the Society and the Santa Clara Valley Chapter of CPMT.

In addition to approximately 70 technical papers over 2.5 days, IEMT '07 will also feature several Short Courses and Vendor Displays. The dates and venue for IEMT '07 will be finalized and announced by October '06.

II. Conference Topics

Paper abstracts are sought from fabless companies, manufacturers (integrated, contract manufacturing service providers) and their Suppliers on their proven capabilities and case studies for package assembly/manufacturing of electronic, solar, opto-electronic, MEMS, bio-medical devices and systems including but not limited to, the following topics :

- Design for Manufacturability: performance modeling of tolerances for cost reduction, reliability standards,..
- Tools & Automation: innovations in bonders, fiber alignment, batch vs continuous (e,g. roll to roll) production
- Manufacturing Systems: metrologies, incoming & WIP monitoring, statistical tools & software (design & process) for QC, predictive models for excursion detection & yield
- User perspective on Outsourcing: impact on cost, logistics, product development ,quality, schedule, supplier selection, on-site and remote monitoring of quality, strategies to create unique products using generic process platforms, IP, licensing, technology gaps
- Outsource Supplier Showcase: turnkey products and services, monitoring systems, in-house development activities, roadmaps for key technologies

Abstracts must be received by **March 31, 2007.** Selected Authors will be informed by **May 15, 2007.**

Selected papers will be due by **August 15, 2007** and should be 5 to 7 pages in length (incl. text and graphics).

For further details visit

www.cpmt.org/iemt/

15th Topical Meeting on Electrical Performance of Electronic Packaging

EPEP 2006

October 23-25, 2006
Scottsdale, Arizona

Sponsors

The IEEE Components, Packaging and Manufacturing Technology Society

IEEE Microwave Theory and Techniques Society

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. We invite your attendance.

Future Directions in IC and Package Design (FDIP'06) – One-day Workshop

Chip Multithreading Keeps the Datacenter Cool – David Greenhil, SUN Microsystems

Carbon Nanotubes: An Emerging Alternative for On-Chip VLSI Interconnects – Kaustav Banerjee, University California Santa Barbara

Characterizing and Managing Variability in Microprocessor Chips – Manjul Bhushan, IBM Corporation

Power Delivery System Design, Modeling and Analysis Challenges for Complex Digital System-in-Package – Zhen Mu, Cadence Design Systems

Future Directions in Computational Electromagnetics for Digital Applications – Thomas Weiland, University of Darmstadt

Electromagnetic and Circuit Co-Simulation and the Future of IC and Package Design – Zoltan Cendes, Ansoft Corporation

Choose from Three Short Courses:

Fast Electromagnetic Solvers for Interconnect and Package Modeling

Power Delivery Networks for Semiconductor Systems: Design, Modeling and Simulation Methods

High- Speed I/O Circuit Design Issues and Techniques

EPEP Sessions:

● Systems ● Measurement and Validation ● TL and Macromodeling ● Noise Containment ● EM ● Power Distribution ● Chip Issues ● Modeling

KEYNOTE TALK: "**The Role of System Integration and Packaging in Future Computing Systems**," Mark Papermaster, IBM

Earlybird registration deadline – Sept. 30th

Conference Web Page: **www.epep.org**

IEEE-CPMT • iNEMI • Georgia Tech Packaging Research Center (PRC) Sponsor the

Second International Workshop on SOP • SIP • SOC (3S) Electronics Technologies

September 28 & 29, 2006

This workshop will review the latest design, R & D and manufacturing status as well as applications of each of the three electronic packaging technologies currently being used around the world. It will also compare and contrast SOC, 3D stacking, SIP, SOP and MCM as related to distinct application sectors.

The preliminary program is now available on the website. Download it today!

For further information and registration, see:

www.prc.gatech.edu/3s

7th International Conference on Electronics Packaging Technology

Shanghai, CHINA
August 26 - 30, 2006

ABOUT ICEPT

Since 1994, ICEPT has been held in Beijing, Shanghai, and Shenzhen, China, every two years respectively. As the only international electronics packaging technology conference organized and supported by the Chinese government and relevant authorities, leading industries and academia, ICEPT has attracted many participants from the whole world, covering all the relevant fields of electronic packaging, such as equipment, ICs, packaging, interconnect, Sensor/actuator/ MEMS/NEMS, Optoelectronics, LEDs, LCDs, substrates, systems, PCBs and assembly.

Sponsored By The IEEE Components, Packaging, and Manufacturing Technology Society, China Electronics Packaging Society, Chinese Institute of Electronics

For registration information and full program, visit:

www.ICEPT.org

IEEE/CPMT 8th International Conference on

Electronics Materials and Packaging

Hong Kong Univ of Science and Technology (HKUST), Hong Kong, December 11-14, 2006

The EMAP conference includes all fundamental and applied science and technology related to the fields of electronic materials, devices, and packaging. Its purpose is to promote awareness of new advances in materials, design and simulations, fabrication, reliability, and thermal management of microsystem/MEMS packages. Also, the technical program will include invited and contributed presentations on theoretical, numerical, and experimental work of electronic materials and packaging. Technical workshops and industrial visit will also be arranged.

Short Courses: **Lead-Free Soldering – Materials, Processes, Troubleshooting, and Reliability**, Ning Cheng Lee; and **3D Integration Technologies – An Overview**, Rajen Chanchani

Keynote Lectures: **Electromigration in Flip Chip Solder Joints**, King Ning Tu; and **Enabling Electronic Prognostics**, Michael Pecht

Papers are solicited in the following Topical Areas:

- Materials and Processing
- Passive and Active Components
- Optoelectronics / Photonics
- Sensor, Actuator, and Transducer Technologies
- Advanced Packaging
- Emerging Packaging Technologies
- Interconnection Technologies
- System-in-Package (SiP) and 3D Stacked Die Packaging
- Electrical Modeling, Characterization, and Signal Integrity
- Thermal-Mechanical Modeling and Characterization
- Packaging Technologies for High Brightness LEDs
- Quality and Reliability

Abstracts Submission Deadline: August 21, 2006

For more details, and the full call for papers, visit our website:

www.ust.hk/emap2006

Coordinate international travel plans to attend one or two other CPMT Society events: **EPTC'06**, 6-8 December, 2006, in Singapore; and **VLSI Chip Packaging Workshop**, Dec. 4 - 5, 2006, Kyoto, Japan.

Call for Papers

TW E N T Y-TH I R D AN N U A L
Semiconductor Thermal Measurement, Modeling and Management Symposium

March 20–22, 2007 San Jose, California

In its 23rd year, SEMI-THERM will include Topic Sessions, Invited Speakers, an Evening Tutorial, and a Short Course program to address key issues highlighted by attendees at the last symposium. SEMI-THERM actively solicits student papers and awards travel stipends and reduced conference fees. Technical workshops, tutorials and vendor exhibits—for which SEMITHERM is well known—will enhance the technical program.

The Program Committee is soliciting papers on current thermal management and practical application issues, modeling and measurement of electronic components and systems in the following areas:

● Practical Thermal Solutions for Low-Cost, High-Volume Systems Design ● Package Thermal Design and Components for High-Volume Semiconductor Packages ● Thermal Solutions for Low-Noise Environments ● System-Level and Board-Level Thermal Design ● .Solutions for Harsh Environments in Commercial, Defense, and Aerospace Systems ● Characterization and Standardization of Material Property Measurements ● Thermal Integration in the Product Design Process, Characterization and Modeling of Thermo-Mechanical Stress ● .Characterization and Modeling of Components, Boards and Systems ● .Temperature and Thermal Property Measurement Techniques ● Transient Thermal Control Methodologies ● .Compact Modeling, Model Reduction and Validation ● .Roadmaps, Specifications and Traditional Cooling

Abstracts are now solicited. The abstract should provide a complete summary of the proposed paper comprising work or result not previously presented or published. The abstract should be between 2 and 5 pages of single-spaced text giving the key results, findings and conclusions, supported by additional pages of figures tables and references as appropriate. Abstracts must demonstrate that proposed papers are appropriate for **SEMI-THERM** and of high technical quality.

Abstracts must be submitted in RTF, DOC or PDF formats via the **SEMI-THERM** web site. Check the web site periodically for updated information.

Abstract Deadline: Sept. 15, 2006

Visit the SEMI-THERM website for the full Call for Papers and additional information:

www.semi-therm.org

For further information please contact the Program Chair via email: Ross Wilcoxon, Rockwell Collins PHONE: +1-319-295-7139 FAX: +1-319-295-3751 EMAIL: rkwilcox@rockwellcollins.com

IEEE/CPMT ASTR 2006

Workshop on Accelerated Stress Testing & Reliability

San Francisco, CA Fisherman's Wharf October 4 - 6, 2006

Accelerated Stress Testing (AST) has been embraced by an ever widening array of worldwide companies seeking to reconcile the need for the highest quality product with the necessary push for early time-to-market. The AST Workshop shares ideas on better ways of accelerating and detecting hidden defects, flaws, and weaknesses in electronic and electro-mechanical hardware that would result in failures during usage. These techniques are focused on testing electronic hardware to destruction limits and root cause investigation to determine the physics-of-failure. The goal of AST is to produce mature products at market introduction and, in making it robust, the product can be screened for manufacturing defects with high combined stresses (beyond end-use specifications) for shorter lengths of time.

Tutorials – Technical Sessions – Exhibitors

For the full program and registration information, please visit our website:

ww.ewh.ieee.org/soc/cpmt/tc7/ast2006

CALL FOR PAPERS

IEEE Polytronic 2007
Conference on Polymers and Adhesives in Microelectronics and Photonics

Miraikan - Odaiba, Tokyo, Japan January 16-18, 2007

Polytronic 2007 will be held at the Miraikan Hall of the 'National Museum of Emerging Science and Innovation', in Odaiba-Tokyo, Japan. The conference provides experts from polymer developers and electronics manufacturers with a unique opportunity for presenting the latest findings, sharing ideas, and learning the fundamentals for R&D of polymer and adhesive materials, and polymer electronic packaging.

During the conference, Japan's largest exhibition "INTERNEPCON JAPAN" is also held from Jan. 17-19 at the same place, featuring materials, equipment and technology for electronics manufacturing, SMT, and packaging, and hopefully may interest you to visit during the conference.

Submission of abstracts: **Sept. 15th, 2006**

Visit the website for the full CFP:

www. polytronic.jp

Papers are solicited in the following areas:

Polymer and Adhesive Materials: Thermoseting, thermoplastic, isotropic/anisotropic/thermal conductive adhesives; underfills, high temperature materials; PCB materials
Processing and Manufacturing: lamination; printing; dispensing; spraying; transfer techniques; underfilling; potting; curing; equipment; SPC; economic analyses.
Low temperatur eprocesses: laminates, bonding, process for non-silicon MEMS.
Reliability and Testing: Degradation mechanisms; adhesion; hermeticity; accelerated testing; humidity and environmental sensitivities; nondestructive testing methods
Functional Polymers for Microelectronics: Conductivity of polymers; electronic transport; polymeric materials for molecular electronics; polymer-inorganic materials interface.
Applications: Polymer electronic devices; polymer optical fibers; polymer wave guides; organic displays; polymer batteries; e-paper; substrates, displays.
Environmental Issues: Ecology and toxicology; life cycle analyses.

2nd Call for Papers **ThETA Conference** – Cairo – Egypt – Jan 3-6 - 2007

International Conference on Thermal Issues in Emerging Technologies – Theory and Applications

θ_1

Objectives: Emerging Technologies in various domains, including Microelectronics, Nanotechnology, Smart Materials, Micro-Electro-Mechanical Systems, Biomedical engineering as well as New Energies, all raise many issues related to thermal effects. The importance of such effects is continuously increasing to a point where they become a dominant factor in determining the performance of such technologies. This is the first event in a series of conferences dedicated to these issues, gathering scientific and industrial communities to exchange experiences, orient research and create cooperation opportunities.

Send a ~1000 words abstract, in any of the following formats: .txt, .pdf, .doc, .sxw to:

thetaconf@gmail.com

Topics:

- Thermal modeling of electronic systems
- Temperature aware computer systems design
- Cooling of electronic systems and data centers
- Micro and nano-scale heat transfer
- Modeling of multiple scale heat transfer problems
- Compact thermal models
- Thermo-mechanical analysis in electronic systems
- MEMS – multi-physics problems
- Computational methods in heat transfer
- Energy conservation
- Fuel cells
- Solid state energy generation / cooling
- Multiphase flow with heat transfer
- Thermal issues in biomedical engineering
- Thermal issues in micro-fabrication technology
- Thermal issues in new materials
- New experimental methods in heat transfer

Call For Papers

57th Electronic Components and Technology Conference

Reno, Nevada, USA May 29 - June 1, 2007

The Electronic Components and Technology Conference is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. The ECTC is jointly sponsored by the Components, Packaging and Manufacturing Technology Society of the IEEE and the Electronic Components,Assemblies and Materials Association of the EIA. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the following areas:

Advanced Packaging: New packaging technologies, systems packaging, density and cooling for single chip, multichip, wafer-level, MEMS and power packages. Special emphasis on flip-chip, fine pitch and high lead count packaging in CSP, BGA, CGA, LGA and SMT packages for both Pbbased and Pb-free bumps and package assembly.

Components & RF: New passive or active component technologies, integrated/embedded components, RF and wireless component applications, modules with subsystem functionality, component performance and reliability.

Interconnections: First-level electronic interconnection technologies including: flip-chip, lead-free interconnect, novel interconnection structures and processes, wirebonding, conductive polymers for interconnect, wafer level interconnect, interconnections for 3D stacking (SIP/SOP), interconnection for new Silicon technologies (e.g. low-k), electromigration of bumped interconnects.

Manufacturing Technology: Advanced process development and equipment improvement for wafer thinning, bumping, stacking; low-k chip and sensor packaging; high-density interconnect and embedded component substrates; testing and burn-in. Cost, yield, performance and environmental improvements, process characterization, design for flexible manufacturing

Materials & Processing: Processes for IC Packaging that enhance performance (mechanical, thermal and electrical) and cost effectiveness, including new technologies, development and application of adhesives, encapsulants, chip underfills, solders and alloys, thermal interface materials, dielectrics, thin films, nano materials to bonding, plating and other assembly processes.

Modeling & Simulation: Electrical, thermal, optical, mechanical modeling, simulation, characterization and packaging solutions including system-level applications.

Optoelectronics: Packaging for fiber-optic modules, optical devices and components including optical amplifiers, lasers, detectors, OEICs, and passive components, nonhermetic and plastic optical packages, optoelectronic package manufacturing and materials, solid state lighting (LED's and display arrays), optical data interconnects,WDMs, and optical back-planes.

Quality & Reliability: Reliability testing and data analysis; failure analysis of field and test failures; reliability modeling of accelerated testing; reliability issues in emerging technologies; interconnect reliability physics, testing and predictive simulation.

You are invited to submit a 750-word abstract that describes the scope, content, and key points of your proposed paper via the website.

Abstracts must be received by **15 October, 2006**.

www.ectc.net

For information, contact Rao Bonda, Freescale Semiconductor,
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