The Electronic Components and Technology Conference - Background Information

Pete Walsh, Arrangements Chairman and Vice Chairman Administration, ECTC

In May of 1950, over 57 years ago, a "Symposium of Improved Quality Electronic Components" was held in the Department of Interior auditorium in Washington, D.C. The motivation for this meeting was expressed by the Chairman of the Steering Committee…..written at a time when many people had not yet even heard of the transistor.

"Most of the modern electronic equipment is made up very large numbers of components….The probability of failure of the equipment is therefore enormously greater than the probability of failure of any one component…. the present industrial situation does not provide (sufficiently) high quality articles plentifully nor do current ideas on permissible size and weight of equipment allow such components to be used generally"

"This Symposium was held for the purpose of inviting a thorough public discussion of the problem within the profession and with the objective of stimulating new effort on the part of component engineers, was well as electronic equipment engineers toward a solution."

The 1950 Symposium was sponsored by the American Institute of Electric Engineers (AIEE), Institute of Radio Engineers 9IRE) and Radio Manufacturers Association (RMA) (now IEEE and EIA) with active participation by agencies of the U. S. Department of Defense and the National Bureau of Standards. It had as a precursor a 1948 Conference on Printed Circuits sponsored by the Bureau of Aeronautics and the National Bureau of Standards. Gil Reid was chairman of the 1948 Conference and Program Chairman in 1950.

There seems to be no evidence that the organizers of the original meeting expected it to become an Annual event. However, its success and the continuing pressure for a forum for engineers to discuss component development and applications resulted in a second symposium in 1952 and annual meetings thereafter. In addition, in 1951, the L.A. Section of the IRE and the UCLA sponsored a Components Symposium in Los Angeles.

In 1954, the Joint Electronic Components Executive Committee 9JECEC) was formed by the sponsoring organizations, to which the Western Electronics Manufacturers Association (WEMA) had been added, with responsibility for management of the annual conferences. This Committee was known as the Electronic Components Conference Coordinating Committee (EC4-now known as the Governing Council). In 1962, WEMA dropped out so that, with the AIEE-IRE merger, sponsorship fell to the IEEE and EIA. The membership of EC4, including the officers, was provided by the administrative committee of the IEEE Components, Hybrids and Manufacturing Technology Society (IEEE-CHMT) and later changed to the Components, Packaging and Manufacturing Technology Society (CPMT) and by the Parts Division (later changed to the Components Group and to the Electronic Components, Assemblies & Material Association of the Electronic Industries Association and later changed to Electronic Industries Alliance (EIA). IEEE/CHMT was formed in 1977 by the merger of the IEEE Professional Technical Group on Parts, Materials & Packaging 9IEEE-PHP) with the IEEE Manufacturing technology Group.

The roles of the Sponsors…The basic role of the sponsors of the conference is to provide operational support and promotion through the resources of their respective organizations. The financial responsibilities are shared equally between the sponsors. Operationally, the sponsors have separate responsibilities as follows:

Administration – The EIA/ECA has the primary responsibility for providing administrative support to the Conference, eg.: coordination of arrangements and operations, by providing the Vice Chairman of Administration responsible for the coordination and general supervision of all Executive Committee functions not associated with the development of the technical program. He works closely with the Arrangements Chairman, Publications Chairman and Publicity Chairman to help insure a smooth running conference.

Technical Program – The IEEE/CPMT Society has the primary responsibility for providing the support to the conference technical program by providing members and leadership candidates for the Conference Program Committee

To give more detail to the above, the EIA/ECA provides support and services for pre-conferences, onsite and post-conference logistics and administration for the conference and technical corner, including site selection and negotiation, pre-registration, onsite registration and administration, and post-conference administration and wrap-up.

Site Selection

- Solicit hotel bids based on Executive Committee city/ies recommendation
- Receipt-review, negotiate and do site inspection/s
- Prepare and present recommendations to the Executive Committee for selection
- Further negotiate, received General Counsel approval and administer contract
- Arrange pre-conference November familiarization tour by General Chairman, Vice Chairman Or Program Chairman, Technology Chairman and Arrangements Chairman

Site Logistics

- Configure hotel meeting space for conference, registration and technology corner
- Establish catering requirements
- Establish A/V requirements
- Request bids and contract for security and temporary services
- Request bids and contract for exhibit management services
- Review/production of all signage including sponsorships, exhibit, registration, session, etc.
- Request bids and contracts for conference shirts, tote bags, etc.

Information Technology

- Monitor, update, and maintain data base
- Monitor, update, and maintain web site (basic)
- Establish secure online conference data base

Pre-Conference Registration

- Receive and process all conference pre-registrations
- Process and verify all payments (checks, wire transfers, credit cards)
- Confirm registration

- Produce badges and onsite materials
- Solicitation of reception, shirt, tote bag, refreshment sponsors, etc.
- Coordinate/produce all conference awards, including plaques, certificates, etc.

Technology Corner

- Prepare and distribute exhibitor manuals
- Assists Technology Corner Chairman with exhibit contractor requirements (re hotel Contract)

Onsite

- Attend onsite pre-conference meeting with hotel to iron out all details
- Set up and supervise onsite registration area
- Develop and administer all guarantees to hotel
- Supervise tote bag suffers
- Distribute shirts to selected members
- Receive and process onsite registration
- Receive and distribute onsite conference materials
- Supervise room setups and A/V requirements
- Position and continually update conference signage
- Supervise hotel accommodations and services negotiated in contract

Post-Conference Registration

- Verify and process registrations (credit cards, etc.)
- Develop and provide necessary documentation on attendees for Executive Committee
- Ship all conference materials purchased, i.e – proceedings, registration packets for Attendees who could not attend, signage, etc.

Accounting

- Process and verify all conference payments and credit cards (exhibitors)
- Process and receive various sponsor and miscellaneous payments
- Prepare monthly reports
- Process and transact revenues and expenses as appropriate
- Develop and maintain all revenue and expense documentation as necessary, including
- Overall expenses incurred by ECA
- Review and authorize revenue and expense invoices as necessary

ECA Incurred Expenses (for reimbursement)

- Conference materials needed for registration and staff office
- Conference print materials needed for sessions, PDCs, registration, etc.
- Postage (regular and overnight)
- Credit card usage fees incurred from AMX, Visa and M/C
- Other items not mentioned above

Off-site/Year-Round Administration

- Planning and contract for November program meeting
- Web site maintenance

Pete Walsh has served the EIA/ECA for the past 38 years ranging from positions of director, marketing services, staff vice president, vice president, and two stints as acting CEO

of the Components Group. In those positions, Mr. Walsh has been providing national membership services and association liaison with Group members, as well as planning and organizing meetings, conferences and exhibitions. Mr. Walsh, for the past twenty-five years, has been Arrangements Chairman, as well as Vice Chairman of Administration for the ECTC.

57th ECTC 2007 General Chair and Program Chair

By Dr. Vasudeva P. Atluri, CPMT Newsletter Editor

Eric Perfecto (SM'01) was the General Chair at this year's 57th Electronic Components & Technology Conference (ECTC) in Reno, NV, and the Program Chair at the 55th ECTC. He served for two years as the Materials and Processes Subcommittee Chair ('02-'03). He has achieved senior member status from IEEE, IMAPS and Society of Plastic Engineers (SPE), and is a member of the Society of Hispanic Engineers (SHPE). He has served as President of the SPE Mid-Hudson section (1993-5, 2001-3) and has been a member of the organizing committee for the "Photopolymers" and the "Polymers in Electronic Packaging" conferences since 1991. He is the Chair of the mentoring committee of the IBM East Fishkill Technical Vitality Council, and for 4 years participated as a mentor for the local high school. He also volunteers as a math tutor for the local junior high school, and has been a frequent judge at the county science fair.

Eric is a Senior Technical Staff Member at IBM, with 25 years of thin films and C4 experience working in the process development of advanced packages at IBM Microelectronics. He holds an M.S. in Chemical Engineering from the University of Illinois and an M.S. in Statistics & Operations Research from Union College.

Eric's technical involvement has been in the development of multi-chip modules (MCM) for IBM's High end systems. There he developed and implemented multi-level thin films technology on top of ceramic substrates. He has led a number of projects in the areas of photolithography, etching, photosensitive polyimide, pattern electroplating and bonding metallurgies for C4 joining, wirebonding and LGA. Through his publications, he led an industry-wide investigation of large format processing to lower the TF cost, and led the development of thin film transfer technology and the optimization of the joining materials (metallurgy and adhesives) and processes (solder and thermoplastic joining). He is currently responsible for the yield and implementation of the C4NP technology. His technical interests include Pb-free solders, chip package interaction, 3D interconnect, and design for manufacturing.

Eric has published over 50 external papers and 12 IBM internal technical reports. He received the 1994 CPMT Trans. - Advance Packaging Prize Paper Award, and the Best Paper Award from the 1st ESTC Conference held in Dresden, Germany in 2006. He holds 30 US patents, has received 3 IBM Patent Awards, and holds the IBM 9th Plateau Invention Achievement Award. He received an IBM Outstanding Technical Achievement Award for the development, optimization and implementation of multi-level thin film modules.

Dr. N. Rao Bonda has been actively participating in the Electronic Components and Technology Conference (ECTC) for several years. He has served as the chairman of the Components and RF sub-committee and has chaired the sessions at the ECTC. He has chaired the ECTC's Professional Development Courses committee and served on the committee for three years. He was the Assistant Program Chair for the 2006 ECTC and Program Chair for 2007 ECTC. He is the Vice General Chair for 2008ECTC.

Rao is currently a member of research and development staff in Freescale Semiconductor, Inc. (formerly known as Motorola's Semiconductor Products Sector) in Tempe, AZ. He received a Ph.D. in Materials Science and Engineering from the University of Pennsylvania, Philadelphia, PA, in 1985. After receiving Ph.D., Rao continued research in materials science at the Ohio State University, Columbus, OH and the University of Wisconsin, Madison, WI until 1989. From 1989 to 1994, he was a research member at IBM T.J. Watson Research Center, Yorktown Heights, NY, and IBM Microelectronics Division, Endicott, NY. In IBM, he developed electronic packages and processes involving flip chip and wire bond chip joining methods, and worked on qualification of several ceramic and plastic packages. His other research work in IBM included failure mechanism studies of Pb/Sn solder alloys to improve the thermal fatigue and reliability of solder joints in electronic packages.

In 1994, Rao joined Motorola's Semiconductor Products Sector in Tempe, AZ, as a team leader for packaging of an optical display module. He developed a fine pitch flip chip bonding process for this display module and improved its yield and reliability through innovative designs. After completion of the display module project, he led new package introductions from design to manufacture implementation and qualified plastic packages for wireless communication and networking systems applications. He currently provides packaging development and technical support for a major wireless communications customer and works with package assembly subcontractors to fulfill the customer's product requirements and packaging roadmaps. He has over 20 technical publications and a US patent.

Rao has been a member of the Board of Governors for the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society for nine years. He was the Chair of its Awards Committee from 1997-2005. Currently, he is the Vice President-Technical for the Society. He is also an Associate Editor for IEEE Transactions on Advanced Packaging journal. He is very active in CPMT Phoenix Chapter and IEEE Phoenix Section. He has served as the chair and program chair for the Chapter and as the treasurer, secretary and vice chair for the IEEE Phoenix Section. He is currently the Chair for the Phoenix Section.

Rao is a member of the IEEE and IEEE CPMT Society. In addition to a Ph.D., he holds an MS and a BS in Metallurgical Engineering from Indian Institute of Technology, Kanpur, and Regional Engineering College, Warangal (India), respectively. He also received an MBA from the Arizona State University, Tempe, AZ, in 1998.

57th ECTC 2007 Sessions Summary

Submitted by Dr. Dave Palmer, IEEE Fellow, Sandia National Laboratories

The ECTC had 250 presentations with 6 given at a time in parallel, as well as 65 posters. One person can only sample a small percentage of the information face-to-face but the proceedings CD or book allow one to catch up after the conference.

In **session 4 on RF Components** Edward Pillai (in picture at left – Edward Pillai presenting in session 4) showed how an upgrade to IBM legacy printed wiring boards were possible using a micro T-coil to match high frequency signals to the existing boards. An improvement from 3 – 12 GHz was possible. Deji Akinwande of Stanford gave a tutorial on parallel and serial RF power combiners/dividers. From this perspective he described a parallel plate TEM mode wave guide that had one input and N microstrip outputs when used as a divider. Li Li of Freescale presented for Lianjun Liu a cavity packaged RF MEMs switch giving 25 dB of isolation up to 40 GHz. The cell phone is one target for this technology. Georgia Tech presented a planar antenna using liquid crystal polymer substrate with embedded resistors that allowed for beam shaping with a large weather antenna as the target. Remco Strijbos of NXP Semiconductors discussed processes that gave high Q ~ 2500 to Bulk Acoustic Filters on solid substrate (contrast with FBAR). Bau-Nan Li of National Sun Yat-Sen University described a miniature band pass filter equivalent to a 3-order Chebyshev using BT laminate and metal traces using only 2.6 x 1.9 mm of surface area. Sandia Labs described passive wireless sensors with 8 bit measurement accuracy which give a 1 milliwatt range of 10 meters based on surface acoustic wave devices.

In **Session 10 on Nanotechnology** Azad Naeemi (in picture at right – Azad Naeemi preparing to talk in session 10 with chair Vasudeva Atluri) of Georgia Tech discussed using carbon nanotubes to improve power distribution on-chip. Combining copper with tubes presents many challenges. Yang Chai of Hong Kong University described the growth of high density arrays of carbon nanotubes with thermal conductivity of 6000 W m / K with the low temperature transfer to another substrate. Rabindra Das of Endicott Interconnect Technologies described materials and processes that would allow embedded capacitors that could be trimmed both by changing dielectric thickness and constant. Chia-Ming Chang of Sun Yat-sen University presented a method of using carbon nanaotubes in polyimide matrix to provide EM shielding to a system. Density of 30% was needed to achieve useful conductivity. Chung-Jung Wu of National Tsing Hua University discussed the mechanical models of conductors that could approach 25 million amps/ cm2. Jiongxin Lu of Georgia Institute of Technology presented the use of nano composites to achieve high-K polymer dielectrics to use as the gate for organic transistors. BaTiO3 with epoxy had been used in the past achieving K=35 but with a high loss. BCB polymer was used this time and

the losses were .016 with K=50. The leakage at 6 V remained small.

In **Session 13 on Wafer Level Packaging** Kai Zoschke (in picture at left - speaker Kai Zoschke with chair Joseph Soucy at session 13) of Fraunhofer IZM presented the next generation of embedded passives on wafers with patterned glass. As a low temperature vapor deposited glass it tested well up to 20 GHz with K=4.3. Won Kyu Jeung of Samsung Electro-Mechanics Co. described a wafer level packaging approach for surface acoustic wave devices resulting in surface mount devices with low stress. The package volume was reduced to 25% of current CSP approaches.

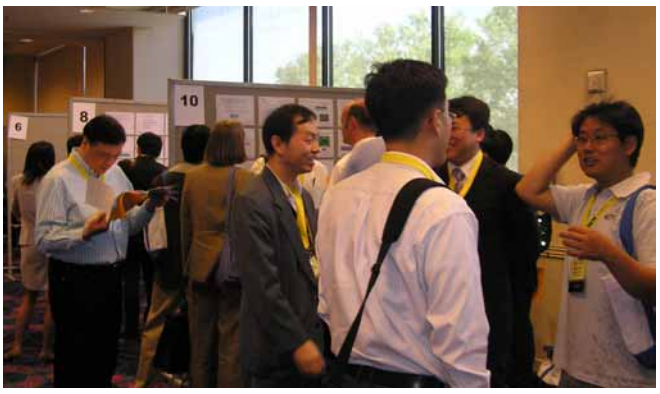
In **Session 17 on Packaging and Assembly Challenges** Li Li of Cisco described minimizing any popcorn effect by careful control of water diffusion over the edge of the chip surface (using seal ring metallization at the edge of die/polyimide interface. Laser dicing was discussed by Taegyeong Chung of Samsung Electronics. In particular the improvement in edge chipping compared to standard sawing of thinned wafers was analyzed. UV laser was not recommended because of redeposit of ablation. Chris Hartsough of University of Maryland described a promising new measurement method to monitor warpage during the increasing complex reflow and assembly steps. Amin Rida of Georgia Tech described an inexpensive coated paper based ink jet antenna for RFID silicon chips. Everyone in the room got excited and had something to ask or add to the presentation…one of those great moments at a conference.

In **Session 22 on RF Modules** A. den Dekker of NXP Semiconductors discussed passive integration on Silicon. His target is the cellular and Bluetooth markets and they develop caps, resistors and inductors. Bo Gao of Hong Kong University discussed low cost passive UHF RFID packaging and the sensitivity to nearby metal surfaces and even moisture in cardboard backing. They developed a ferro antenna that isolates the EM from the backing so they can have an on-metal tag. George White of Jacket Micro Devices presented GURU (Global Universal Radio Units) and the process to obtain high Q passives using organic multilayer board to come up with an inexpensive alternative to the LTCC approach. John Park of Cadence described a complete family of RF silicon in Package design tools recently developed with the strong financial backing of 3 of their clients.

In **Session 25 on MEMS Packaging** Mark Wagner of Sensorcon described using packaging materials not silicon to give low cost MEMS package that will not be integrated directly on an IC. Suk-Jin Ham of Samsung Advanced Institute of Technology described a wet etch high resistivity silicon cavity package to protect FBAR structures from further oxidization. The package was sealed in nitrogen at 260 C with AuSn solder. Tests were done at 2 GHz.

In **Session 27 on Nano, Bio and RF** Matt Lueck (in picture at right column top – Matt Lueck presenting in session 27) of RTI International described a silicon interposer with embedded through wafer inductors. The interposer with passives would be positioned between two face –to-face ICs. 400 micron thick wafers were used with Bosch etching and copper metal to achiever Qs of ten. Frank Theunis of NXP Semiconductors described customer RF MEMS package family with nitrogen back filling. The cavity is only 3x3 mm. SnAu solder seal is only 80 microns wide so it does not provide large parasitics with the I/Os. Chien-Hsiang Huang of National Sun Yat-sen University showed a modeling design system that could achieve Qs of 100 with both LTCC and thin film processes in the L band. This work was done with closed form formulas not fancy workstation numerics. Hanyi Ding of IBM described the design and testing that went into entering a millimeter wave general Wilkinson divider into the IBM library. The confirmation testing was done at 94 GHz.

In **Session 31 on Advanced Packaging** Moody Dreiza of Amkor Technology described a high density Package on package with a top memory on a bottom logic package. Known good units had to be used for the high volume cellular market. "Dipping Paste" was used on solder bumps to help compensate for any warpage. Kazuo Ishibashi of Nokia Japan talked of warpage on PoPs and minimizing yield loss. Kai Liu described technology for many RF modules intended for WLAN market. The approach was to have many chip scale modules that could be used as building blocks for any application needed to provide quick product cycle time. Cher Bai of Qualcomm described the analysis using die size, thermal via count, and amount of copper on board to predict the thermal performance of modules for mobile handsets. Tae Kyun Kim of Samsung described screen printing in a high vacuum and how this is better than glob top for System-in-Package applications. Raj Pendse of STATSChipPAC discussed extremely thin wafers and using flip-chip. Even removing bumped chips from tape after singulation proved challenging. Three stacked chips on BGA (.24mm) resulted in only 1.4 mm thickness after molding.



Lots of excitement at Poster Sessions

57th ECTC 2007 Invited Sessions and Meetings Summary

Submitted by Dr. Dave Palmer, IEEE Fellow, Sandia National Laboratories

Luncheon Keynote:

Jeff Jonas of IBM Las Vegas gave a titillating ECTC lunch speech. He presented several proven techniques to defraud casi-

nos of more than $100,000 in one hour. We all had to promise not to divulge this information so this article will remain vague on details.

Jonas is an IBM distinguished engineer who has written the book "Cheating Las Vegas." His main theme for this talk was that you must treat your data like a question or you will never know its relevance unless someone just happens to ask the right timely question. He described NORA (Non-Obvious Relationship Awareness) as a set of software that takes many databases and "asks" questions that result in important correlations.

One example presented was that there are 38 million visitors a year to the 20 largest Vegas hotels. Enough data exists at the hotels that with the proper data mining software they could have prevented the few thousand known cheaters and thieves in this 38 million from entering their doors. However, today they only find out about the correlations after the criminal has left. Jonas defined this as Enterprise Amnesia, where one part of the company has data needed by another but never asked for. Each year many people are hired by a casino that were arrested in past years for committing crimes at the same casino. Many more are hired who are related to such criminals or are suppliers of critical supplies to the casino. Many conflict of interest issues are actually "known" in the casino data archives.

He pointed out one weakness of slot machines (that is now fixed). When a new $100 bill was issued it could not be read right by the slot machine so it would give the correct amount in tokens plus give back the bill. He also showed a little light emitting stick that could allow a slot player to empty all the coins in the machine no matter how minor the actual win.

Another term he introduces was "perception isolation." The cure was to run all kinds of cross checkers (ask the right questions) every time new data is entered. For example, notice that D. William Banks used to work at the casino and was fired and now David W Banks has just interviewed. So each piece of data is really a set of data base queries and each query should find related queries. If ten different queries are generated in the last week on some variations of D. W. Banks this is probably not coincidence but should be investigated.

Jonas described one application of these software ideas concerning the effort to reunite New Orleans residents after the Katrina Hurricane. They entered 1.5 million Internet postings for missing people. Reduced this to 38,865 unique real persons (there were many redundant or fake entries). This resulted in more than 100 families being reunited (some matches did not want to reunite and many were false matches).

He stressed that as computer power and storage is growing we are often ironically getting dumber. The right automatic query tools help but privacy must also be protected. He described a future Analytics in an Anonymized Data Space. Using this, many government agencies or casinos could compare databases in an encrypted memory bank so that no one person could see all the data. However, if the D. W. Banks showed up in numerous data bases with a dark cloud then the Software could suggest to each data owner that they have reason to ask particular other data holders about "Banks". At this point human judgment can enter the picture.

After his talk there was a rush to both Radio Shack and the casino.

CPMT Seminar:

In Reno at ECTC the CPMT seminar was held Thursday evening, May 31. The subject was "Advanced 3D Packaging Technologies" and the meeting was chaired by **Yoshitaka Fukuoka** of Weisti and co-chaired by **Kishio Yokouchi** of Fujitsu Interconnects Technologies, Inc. The meeting room was packed and so were the viewgraphs. For those that need the details it would be best to obtain copies of the visuals either from the speakers or from the "members only" section of the CPMT web site.

The first speaker was **Haruo Shimamoto** of Renesas Technology Corporation with "Technical Trend of 3D Chip Stacked MCP/SiP." He saw SiP as the driver of advanced packaging as a result of the increased I/O count, the higher data transfer rates (particularly from memory), need for less delay in data paths, and need for small volume. He saw flip-chip growing in popularity for SiP, continued improvement in through silicon vias for chip stacking, and a general expansion of 3D packaging.

Hiroaki Ikeda of Elpida Memory addressed "3D Stack DRAM using Through Silicon Vias." The driver for this industry is the need for x3 speed improvements in memory every 2 years and the need for x2 bits every 2 years. Clever stacking has been able to give the system designer the memory needed 6 years before Moore's law makes a monolithic solution possible. So the design goal is to stack while simplifying the data paths. He presented 8 memory chip layers in a stack with the internal bus connections. Where necessary interposers from Oki were used between layers. He discussed placing high temperature resistant poly-Si vias in the wafer before any transistor processing was performed (via first). To minimize the amount of poly needed the process leaves Si posts in the via which is about 28 microns in diameter resulting in 4 ohm resistance. Larger vias are made for power distribution. There is a redundancy of vias so that a circuit can be repaired if one via connection is substandard.

Naotaka Tanaka of Hitachi presented "Silicon through-hole Inter-

connection for 3D-SiP Using Room Temperature Bonding." His goal was heterogeneous stacking; a mix of memories and microprocessors. These vias were copper to achieve low resistance. The processes were designed to use existing equipment but the mechanical caulking method developed was new and used compressive pulses to deform the copper bumps into the laser drilled vias in the wafer. He claimed that even with 7% of the chip becomes vias it is still not fragile and can be handled with normal production equipment. Final assembly was possible using 10 micron alignment accuracy.

Yasumitsu Orii of IBM Japan discussed "Ultra thin PoP technologies with 50 micron pitch Flip Chip C4 Interconnection." The mobile phone push to have a TV option is pushing this technology, because they can add functionality and still keep the necessary thinness. The motivation for this research is the better yield of flip-chip on PoP than with wirebond on BGA. The process was developed so each package can be tested before assembly. He went into detail on the solder on copper post technology used where the crust of the solder is controlled so it helps the yield. This technology takes 3 years for IBM to qualify.

Katsumi Kikuchi of NEC Corporation presented "a High-Density SiP Technology for Inter-Chip Wide-Band Data Transmission. A technology named SMAFTI was developed for SiP to give high data transfer rate from memory to logic. Silicon was used for most layers to keep CTE match possible. For example the interposer was a 15 micron thick silicon patterned chip with the memory on one side and the logic on the other.. Copper vias 10-20 microns in diameter were used. Much development went into the resin overmold material and process to be compatible with the rest of the system.

ECTC Plenary Session:

The ECTC Plenary session was held Wednesday night, May 30, chaired by Wolfgang Sauter of IBM Corporation. The Panel theme was "Where does Packaging Research and Development take place: Current Trends and Production."

Wolfgang Sauter set the urgent tone by noting: (1) the cost of packaging must always go down, (2) outsourcing of assembly is increasing, (3) packaging complexity is increasing, and (4) one big source of packaging research, North America, is decreasing in publications at a rate suggesting "zero" research by the year 2032. (Fortunately most in the audience quickly realized they would be retired by doomsday).

Mostafa Aghazadeh

First, Mostafa Aghazadeh of Intel addressed where development will occur. The main driver is that critical tech development occurs where the suppliers are located, such as that needed for high density flip chip. The other driver is in competitiveness; costs are lowered by development/designs in geographies where customers vote.

He used an "Ecosystem" model. Just as many semiconductor companies were driven by cost to go "fab-lite", he suggested that a market with a broad set of specialty packaging technology vendors could provide better solutions than the past in-house solutions.

Mostafa predicted continued strong growth in both the chip and assembly business through 2010. He saw increased R&D by the assembly subcontractors in order to give them a market edge. However, with the increased cost of technology and complexity of assemblies, the push will be for more efficient use of R&D funds. This will lead to: (1) an improved model for collaboration in technology development, (2) a push of R&D upstream in the value chain, and (3) leverage consortium to derive a common agenda.

He predicted ever increasing interaction between wafer fab and packaging technologies as the scaling, Low-K, System-on-chip, and wafer level packaging trends continue. The boundary between fab back-end and assembly front-end may not exist anymore. Particular emphasis will be on thinning and bumping.

Geographically he sees the continued flight of electronics to Asia: assembly went in the 60s and 70s, fab lines in the 90s, and now system design. He pointed out that salaries in India and China are 25% of North America and that Asian countries produce 4 times the engineering grads.

Rao Tummala

Next Rao Tummala of Georgia Tech discussed the roles of universities in this R&D adventure. First is exploring all technology possibilities with a 10 year horizon. Although most will not reach production, it is important to consider all options. Second, the universities must educate the next generation of packaging engineers with (1) system perspective, (2) global view, (3) cross-disciplinary knowledge, and (4) leadership skills.

Rao pointed out that there were 50 universities active in packaging in North America, 35 in Europe, and 65 in Asia. These numbers had greatly expanded from the 1970s when most universities only studied circuits and silicon transistor fabrication. He pointed out that university work included blue sky and strategic research as well as technology development.

Rao emphasized SOP, system on the package, which combined the best of system and IC integration. However, today further IC integration only accounts for 10-20% of system size diminution. Whereas system integration (passives, antenna, power, interconnect) is the major driver.

Rao sees universities as complementary to the necessarily shorter future focus of industry. He pointed out projects at Georgia Tech supported by 50 companies. He pointed out Sony, IBM, and Intel as good partners for mutual research despite their past history of excellent vertical integration.

On a visionary note, Rao Tummala declared "miniaturization brings everything else." Going from today's cell phones that do about 10 different functions (audio phone, camera, voice recorder,

music play back, text message, gps, Internet e-mail), he projected in about a decade we would have affordable electronics systems of 5 cc volume with a million functions. To reach this goal, the weakest link to be strengthened is system packaging.

Wayne Howell

Next Wayne Howell of IBM discussed leveraging packaging technology for product innovation. He stressed we must have a Business Model innovation to make progress. There must be an efficient way to optimize the assets you have and the assets you must partner for. A business model must give guidance on when/how to partner and when to go it alone.

Wayne stressed the mantra "A package is a happy home for a chip" with the I/O as the only functional connections. His rules for the packaging engineer were:

1. Do no harm
2. Be transparent – as simple as possible
3. Enable more performance from the chips
4. Provide unique capability – build a market edge

The Howell taxonomy:

If it is possible it is exploratory research.
If it is useful it is technology development
If it is called product integration than it can be manufactured

Wayne Howell stressed that many companies were very innovative but few were on all three needed fronts: technology level, manufacturing level, and business level.

Robert Darveaux

Lastly Robert Darveaux of Amkor underlined much of what the previous speakers indicated but he emphasized that a better Intellectual Property model is needed to foster quick, effective cooperation between potential package development partners. He listed a number of attempted cooperations that were scuttled by lawyers because the legal structure for IP was not mature in our industry.

Robert Darveaux also stressed that the business model is just as hard to innovate, maintain, and grow as the technology efforts most often discussed at ECTC. However one particular technology challenge facing industry is the testing of product with many functions and many layers of software.

ECTC President's Panel:

An exciting panel session occurred Tuesday May 29th at this year's ECTC. President William Chen led a discussion of future electronics technology entitled "When technology Meets market: More Moore and More than Moore." The large audience slowly figured out the title as the evening proceeded.

Chen pointed out that Moore's original article not only predicted that the number of transistors on an IC would periodically double but he predicted that complex electronics would be sold in department stores (this was before the term "big box stores" was coined. He also pointed out that economists look at the $1.4T share electronics has in the economy and see it as about the seventh largest contributor globally.

Bob Sankman

Bob Sankman from Intel started the discussion with the status of 45nm CMOS IC technology, "Challenges in 45nm and Beyond". He reviewed the start of 130nm in 2001 and suggested 45nm will begin in late 2007 – showing that the number of transistors are still doubling every 2 years.

To package this technology it will take the equivalent of 100 C4 bumps per square millimeter, which has proven possible. However, scaling pins at this density for 45nm will not be mechanically practical because of fragility. Bob made it clear that it is important for substrate experts to optimize very high density features to help solve this packaging challenge.

The substrate may also need low-K dielectric material. This will increase a problem since Low-K are mechanically weak materials and the many small bumps will bring high stress.

Another concern is that the next generation of ICs will have even more localized heating as groups of transistors switch fastest in one location or drive the longest lines in another location. To date heat spreaders and sinks treat chips as isothermal planes.

Lastly, packages are desired to be thinner. Thinner implies more warpage unless much more process and material development occurs. Design tools need to include signal integrity monitors while developing routing in the package.

Despite these hurdles for 45nm packaging, Bob Sankman saw no "show stoppers" even for the next step of 25nm CMOS.

Brandon Prior

Next Brandon Prior of Prismark spoke of high production volume systems that will drive the future with the title "Games Systems and Packaging Technology". Brandon felt that many of the packaging solutions are in place for next generations. Unlike cell phones, the game industry is producing product with X2 in size and X4 in weight from the last generation. This more powerful generation produces more heat and is still obeys the limitations of lower cost printed wiring boards.

Each generation lowers its price as it is revised. Silicon integration does take place to help lower costs, but the packaging challenges remain. Typical approach uses BGAs with an internal flip-chip. They use 200-250 micron bump pitch which is well established. For cost the BGA has a copper heat slug or a heat pipe. In general the game units get hot. Memory is sometimes within graphics processor package for speed. One recent challenge has been the evolution to Pb-free. SnAgCu solders are used.

The AMD/ATI fusion has influenced the game market. They are using the one package with many chips solution where possible. In addition, much integration to silicon is taking place.

Prior predicts that the tablet PC as the next killer application. In this case size and weight needs will require better board technol-

ogy. HDI-type technology adapted from mobile phones perhaps. The PoP, packaging on package, approach will be used where a memory stack is placed on top of a wire-bonded large die.

Petri Savolainen

Next Petri Savolainen representing Nokia in Finland presented "Packaging for Mobility, Intelligence & Style." He suggested something that the engineering audience had trouble accepting, namely that consumers often decide on which cell phone to buy based on "style" and not necessarily the best functionality.

He pointed out that the phone is becoming a computer to get e-mail and is taking on other functions such as photography. These increased abilities are often the goal now that the size race is no longer the main decider. Even though the size/weight is no longer the sole metric, "you can never be too thin."

Advanced Packaging is still the key to each generation of mobile phones. The quest for more phone intelligence is resulting in die stacking, package-on-package, and package embedded ICs. Tomorrows phones will need faster ICs which do not need larger batteries. The phone is the internet link most of the time for more people.

Given all this exciting component and packaging challenge, Savolainen reminded the audience that success in this arena without having your product make a fashion statement and passing the "looks cool" test would result in a business failure.

Herbert Reichl

Prof. Herbert Reichl of IZM Germany presented a "Research vision for More Moore and More". He discussed the European Technology Platform work labeled "Nano-electonics" but indicated that the whole advance electronics effort would be better called "heterogeneous Integration". By this Reichl meant the expansion of the system packaging to include batteries, antenna, and sensors. It would be a smart system with some components made "package-sized" by the use of nano-materials: advanced cooling, low-temperature interconnect, and self positioning.

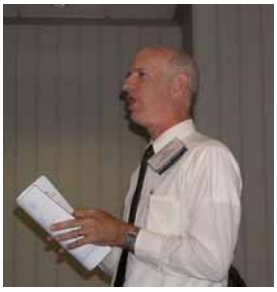
Reichl showed the "old" digital IC as only a part of the system with wireless, power supply and sensors also being integrated on the chip. He saw more of the historic "packaging" taking place at the wafer level further blurring the "back-end" from the assembly. He agreed that thinner was a continuing theme.

On the module level he saw polymer build-up technology with embedded passives not unlike the BCB-Cu technology that was popular a decade ago before the tech crash. He also saw the packaging build the battery layer by layer as the rest of the package was fabricated.

CPMT Publication Quality Strategy Meeting:

Early Friday morning at 57th ECTC 2007 meeting in Reno, Nevada, a CPMT Publication Quality Strategy meeting was led by Avram Bar-Cohen and Paul Wesling to improve Publications quality.

President William Chen set the tone for the 15 attendees stating: (1) we have improved the official impact metric of our Transactions over the last few years but they can become greater for all members benefit, (2) today's article cycle time can be slow and articles have been lost, (3) a lot of the quality of CPMT to our profession comes from our quality publications, and (4) as activities continue to move to Asia we must strive for more Asian reviewers, editors, and readers. "We are never too proud to improve."



Paul Wesling added that our publications serve a large community (80,000) in addition to our society members (3000). However, since IEEE Xplore Internet access to articles is virtually universal, we must optimize our quality for our much more transparent community.

Avi Bar-Cohen enumerated and facilitated discussion on the publication challenges. Since packaging science and engineering are intertwined, our Society must be a home for both the practitioners and the academicians. Often practitioners want immediacy and novelty in publications whereas professors are driven by citations and journal "impact factor". We must benefit both, since publications are key to the CPMT "value proposition."

IEEE Transactions expectations are (1) half of manuscripts finish first reviews in 3 months, and (2) No manuscripts are laggard for more than 12 months.

Our Transactions were born more than 60 years ago. Two reformulations in 1994 and 1999 resulted in our 3 current transactions:

- Components and Packaging Technologies
- Advanced Packaging (partnering with LEOS)
- Electronics Package Manufacturing

Each year 400 manuscripts are submitted and about 300 are published taking about 2100 pages to 5000 subscriptions. In addition, articles are called up by subject searches using Xplore.

A journal's "impact" is determined by the number of times its articles are referenced within two years after publication. Clearly the impact goes up if results are published quickly so others in the field have your current work, if other authors to our Transactions are aware of previous similar articles in the same Transactions (90% of references to our Transactions are in other journals), and if our articles are filed by the best descriptive titles and key words so they are found in computer searches.

Attributes of a High Impact paper: