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- Original contribution of data, understanding, techniques, or process
- Furthers state-of-art
- Removes barriers for implementation
- Previously unpublished work
- Sufficiently detailed so the work can be repeated
- Clearly identifies prior art and how this work builds on that
- Written in proper English
- Right words in title and key word section so it can be found
- Clearly implemented so review process will go quickly

The path of the manuscript takes about 6 months from submittal to the mailed out Transactions. Quick response by the editors and authors can cut a bit of time from this but this remains the goal because typically busy schedules add some time to the process. To increase the value of the Transactions our Society will add an IEEE staff person to bird-dog the manuscripts. Editors will help authors with higher impact titles, references, and key words. Many of our best written communication remain in the "non-archival" conference Proceedings which does not have the reach and completeness of the reviewed/edited Transactions. It is hoped that these quality improvements will entice more conference presenters to do the extra work to help the profession through a Transactions paper.

Components and RF/Wireless TC meets:

Your Technical Committee concerning RF and Wireless as well as your ECTC committee covering Advanced Components and RF met for a breakfast meeting under the leadership of Mahadevan Iyer, Georgia Tech. Ten volunteers attended and Craig Gaw contributed over the speaker phone. Attendees included: Lih-Tyng Hwang, Tim Lenihan, Nanju Na, Hideki Sasaki, Len Schaper, Eric Beyne, Amit Agrawal, J. J. Maloney, and Dave Palmer.

This group is responsible for attracting many RF and Component papers for the ECTC meeting as well as for the Transactions. The sessions chaired by this group had about 100 attendees. It was stressed at the meeting that authors must submit advanced component papers through this group and not just RF component papers. The goal is 45 papers.

Nanja Na, J.J. Maloney, Hideki Sasaki, Lih-Tyng Hwang, and Mahadevan Iyer at Components and RF / Wireless TC Meeting

A list of past authors, future possible authors, and organizational volunteers was again updated in preparation for another year of ECTC preparation and member communication. A call for papers for the next ECTC was outlined with the final being released soon by Craig Gaw and Mahadevan Iyer. Some of the topics to emphasize were integrated passives processes and yield, high performance discretes such as decoupling capacitors, and high frequency modules.

Workshop Reviews:

Summary of the 10th European System Packaging Workshop Como, Italy

January 29th-31st, 2007

www.packagingworkshop.polito.it/

Submitted by Evan Davdison, IBM (Retired)

The Technical Committee on Systems Packaging had a very successful workshop in Como, Italy last January. Fifty-eight people attended. Most were from Europe with significant contingents from Asia and North America. It was a thorough program including topics on: wearable electronics, medical devices, portable equipment, 3D packaging systems, high-speed optical communications, electromagnetic simulators, microprocessor packaging, computer systems, process technologies, MEMS and market analysis. This breadth of papers was typical for a Systems Packaging workshop (the full program can be seen at the above website).

TCSP workshops focus on the need to integrate all aspects of an electronic system to create a product. Throughout its forty-year **history**, TCSP has been doing this. In this age of non-vertically integrated companies, external component vendors, contract manufacturers and outsourcing; our mission is especially important. The company that markets the final product has to create the system design, procure all the parts, build the prototype and be responsible for functionality, design integrity, design aids, component specifications, qualifications, cooling, and overall reliability. TCSP workshops are unique in the sphere of technical meetings by providing an emphasis on gluing all these total systems technology elements together at the final product level. Quite often the role of hardware integration falls to the system package designer and it is the needs of these people that TCSP meetings address.

The 10th European Workshop was chaired by Flavio Canavero (Politecnico di Torino) and Carlo Cognetti (STMicroelectronics) with help from Flavio's able assistant, Carla Giachino: the treasurer and logistics expert. Thomas Winkel (IBM Germany) and Cian Ó'Mathúna (Tyndall) were the Program Chairs. There were seven keynote presentations from the following well-known experts: Madahavan Swaminathan (Georgia Tech), Herb Reichl (Fraunhofer IZM), Len Schaper (U. of Arkansas) Carlo Cognetti (STM), Bob Guernsey (IBM USA), Christian Val (3D Plus) and Jan Vardaman (TechSearch USA). Some of these and other presentations can be seen at the workshop website.

There was a multitude of advanced work presented at this workshop. Most of it is already in products. Some of the key take-away points are:

- Thinness and low power in portable devices are new key drivers for semiconductor and packaging technologies.

- Computer, networking and telecommunication products are still driving performance and technology complexity for both semiconductors and packages.
- Embedded passives and optical waveguides on packages with on-chip electro-optical devices is finally ready for primetime.
- 3D packaging with through-hole vertical silicon vias and bump connection technology is making thin products even thinner.

The website contains many of the paper abstracts and presentation slides. To fully understand the comprehensiveness and value of this workshop, we encourage you to have a look.

Needless to say, Lake Como was a beautiful serene place to meet people and have a workshop that taught us so many new things. The next European workshop will be held in 2009 at Blarney, Ireland in County Cork: another wonderful place to learn and meet new friends. The 2008 Japanese TCSP workshop will be held in the beautiful Hakone resort region of Japan.

Check at the TC website (www.ewh.ieee.org/soc/cpmt/tc14/) for upcoming information.

Chapter Reports:

Backend Wafer Processing Technologies

Submitted by Dr. Mali Mahalingam, Tutorial Committee Chair, IEEE CPMT Society Phoenix Chapter

This half-a-day tutorial was taught on behalf of IEEE CPMT Society Phoenix Chapter on April 18th 2007. Dr. Mali Mahalingam, chair for the tutorials technical program worked with his fellow Phoenix CPMT officers in organizing this totorial. Four major areas of ***Backend Wafer Processing Technologies*** that precede and enable backend assembly and packaging were the focus of the tutorial. Forty six professionals took advantage of this professional learning opportunity.

Stacked Die Packaging and many consumer applications are driving ***Wafer Thinning*** technologies relentlessly. High performance applications demanding excellent thermal, electrical and mechanical performance for die attach are making continuous demands on ***Wafer Backside Metallization***. Flip Chip interconnect assembly is pervasive in high performance applications and now expanding to consumer applications thus propelling further growth in ***Wafer Bumping*** technologies. Numerous new challenges have arisen in ***Wafer Dicing*** due to use of Cu metallization and low-K dielectric materials in wafer fabrication. Each presenter presented an overview of basic technologies, discussed current challenges, and offered solutions in their respective areas.

Mr. Scott Drews, a Senior Applications Engineer for SEZ America, Inc. presented the topic of **Wafer Thinning.** As consumers demand greater product functionality in smaller packages, device manufacturers look for ways to integrate, through system-in-package (SiP), system-on-chip (SoC) and stacked die packaging. In order to maintain low die profiles in stacked die packaging, most manufacturers target final silicon thicknesses below 100um. While several methods exist for wafer or die thinning prior to packaging, manufacturers must take into consideration issues relating to process integration, waste abatement, reliability, die yield and cost-of-ownership when selecting which method (or combination of methods) to implement.

Dr. Jonathan Harris, President of CMC Interconnect Technologies, presented the topic **Wafer Backside Metallization.** Backside metallization of semiconductor devices followed by solder based die attach results in a die bond with excellent thermal, electrical and mechanical properties. The presentation focused on the back-side metallization of semiconductor wafers to achieve this type of high performance die attach. Both silicon and GaAs devices spanning applications in RF & Microwave, Power Control and Optical Devices were discussed. Various backside metallization systems, the design attributes for these metallization systems and the material science behind achieving key back side metallization requirements for each application were discussed. Deposition technologies including sputtering, evaporation and plating technology were discussed and compared.

Mr. Ted Tessier, Chief Technical Officer at Flip Chip International in Phoenix Arizona presented the topic of **Wafer Bumping: The Past, The Present and The Future.** After a rather lengthy period of development and adoption for high performance computing and automotive applications, wafer bumping and flip chip assembly technologies are now rapidly being accepted for use in consumer electronics and handheld communications applications. From these initial Flip Chip in Package beginnings, a number of bumping technologies have emerged to support a wide range of semiconductor device requirements and packaging applications. This presentation provided an overview of the history of wafer bumping technologies including the adoption of thin film redistribution options to broaden the applicability of wafer bumping to ICs designed with wirebond centric peripheral pad arrangements. The emergence of Wafer Level Chip Scale Packaging (WLCSP) was discussed and the differences between flip chip and WLCSP bumping technologies were compared.

Mr. Alan Magnus, a Member of the Technical Staff at Freescale Semiconductor Inc. in Tempe, Arizona, presented the topic of **Wafer Dicing.** The drive for low cost microelectronics with enhanced electrical performance has introduced wafer fabrication materials and advanced packaging requirements that present an ever increasing challenge for the wafer dicing operation. Some complications stem from the wafer fabrication materials such as multi-level interconnects of Cu metallization and low k interlayer dielectric materials. Packaging constraints play a role through die thickness and mechanical strength requirements, as well as bumping or back metal needs. Finally economic issues, whether reduced scribe widths to increase the number of good die per wafer,