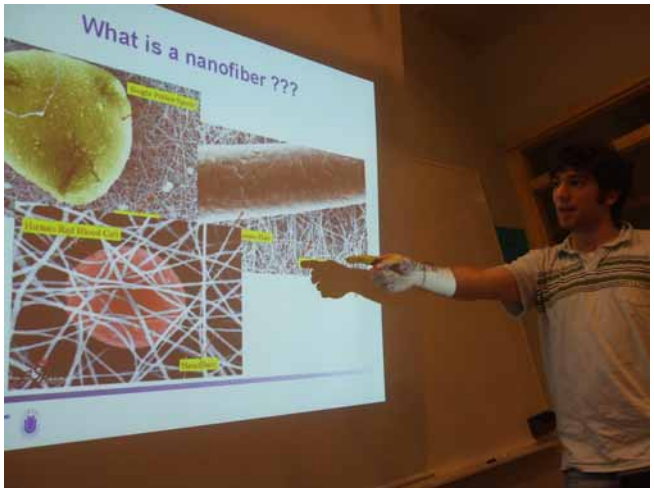
Guest lecture about MEMS from Iomega during October, 2007 for the student members of year 2007 / 2008

Professor Johan Liu is discussing with the student members of year 2005/2006 during Project Seminar held in March, 2006

Project Seminars during January thru April, 2007



Student members of year 2006/2007 are presenting

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Conference Reviews:

58th Electronic Components and Technology Conference (ECTC) Update

Submitted by Dr. Rajen Dias, Asst. Program Chair

The 58th ECTC that will be held at Disney's Contemporary Resort in Lake Buena Vista, Florida, USA during May 27 to 30, 2008, has received 616 technical abstracts, a record number for the technical program. The technical program will feature over 300 high quality technical papers, presented in 36 oral sessions, two poster sessions and a special student poster session. The papers will cover a wide spectrum of topics including advanced packaging, interconnections, electronic components, materials, processing, assembly, manufacturing, optoelectronics, quality and reliability, modeling, simulation and emerging technology that focuses on nano-technology, biomedical and flexible electronics.

The technical program is complemented by 16 professional development courses, a plenary session, a panel discussion session and a CPMT seminar session. In addition, there is a technical exhibit corner where over 50 leading companies, primarily in the electronics components, materials, thermal and packaging fields exhibit their latest technologies and products. The conference allows ample opportunities to network and meet leading experts in the field.

For more information on 58 ECTC, please visit **www.ectc.net**

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ECTC 2008 Professional Development Courses Tuesday, May 27, 2008

Kitty Pearsall, Chair — ***IBM*** — ***kittyp@us.ibm.com*** — ***+1-512-838-7215***

Jeffrey Suhling, Co-Chair — ***Auburn University*** — ***jsuhling@eng.auburn.edu*** — ***+1-334-844-3332***

Vasudeva P. Atluri — ***Intel Corporation*** — ***vpatluri@ieee.org***

Goran Matijasevic — ***University of California, Irvine*** — ***goran@uci.edu***

(continued…)

Morning COURSES
8:00 AM - 12:00 PM

1. ACHIEVING HIGH RELIABILITY FOR LEAD-FREE SOLDER JOINTS - MATERIALS CONSIDERATION

Course Leader: Ning-Cheng Lee – Indium Corporation of America

Course Objectives:

This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail, and novel alloys with reduced fragility will be presented. Electromigration, corrosion, and tin whiskering will also be discussed. Furthermore, the reliability of through-hole solder joints will be reviewed, and recommendation will be provided, particularly for thick boards. The emphasis of this course is placed on the understanding of how the various factors contributing to the failure modes, and how to select proper solder alloys and surface finishes for achieving high reliability. Also will be presented are the desirable future alloys and fluxes in order to meet the challenge of miniaturization.

Course Outline:

- Implementation Status
- Prevailing Materials - Alloys and Finishes
- Surface Finishes Issues - ENIG, ImAg, and ImSn
- Mechanical Properties - Shear, Pull, and Creep
- Intermetallic Compounds - Effect of Cu, Ni, Other Additives, and Heat History
- Failure Modes - Grain Deterioration, Orientation, Mixed Alloys, and Interfacial Voiding
- Thermal Cycle Reliability - Effect of Cycling Condition, Surface Finishes, and Reflow Temperature
- Reliability of Through-Hole Joints - Large and Thick Boards, Partially Filled Through-hole
- Fragility - Effect of Surface Finishes, Alloys, Reflow, Strain Rate, Aging, Cycling, and IMC
- Electromigration - Effect of Current Density, Back Stress, and Cu UBM Thickness
- Corrosion - SAC and Performance of Surface Finishes Under Harsh Conditions
- Tin Whisker - Causes of Formation, Methods for Control

Who Should Attend:

Any one who care about achieving high reliability lead-free solder joints and like to know how to achieve it should take this course.

2. ULTRAHIGH THERMAL CONDUCTIVITY PACKAGING MATERIALS

Course Leader: Carl Zweben – Thermal Materials Consultant

Course Objectives:

This course provides an in-depth discussion of the increasing number of ultrahigh-thermal-conductivity materials that address key packaging problems: heat dissipation, warpage and fracture of low-k dielectric layers, solder joints, etc., arising from differences in coefficient of thermal expansion (CTE). Topics include properties, manufacturing processes, applications, cost, lessons learned, and future directions, including carbon nanotubes. Traditional materials are included for reference.

There are now over 15 low-CTE, low-density materials with thermal conductivities ranging between that of copper (400 W/m-K) and 1700 W/m-K. Thermally conductive carbon fibers allow heat removal from the bottom, as well as the top of a chip, expanding the range of convection cooling. The fibers also can tailor substrate and printed circuit board (PCB) CTE, potentially eliminating the need for underfill. Carbon nanotubes and fibers can greatly increase thermal interface material thermal conductivity. Low-CTE solders under development will provide additional advantages.

Advanced materials are being used in an increasing number of commercial and aerospace microelectronic and optoelectronic applications, including servers, laptops, phased array antennas, telecommunication equipment, laser diodes, solid state lighting, plasma displays, liquid crystal displays, etc. For example, low-CTE diamond particle-reinforced SiC heat spreaders having a thermal conductivity of over 600 W/m-K were used in IBM servers.

Course Outline:

- Key heat dissipation, thermal stress and warping problems
- What is wrong with traditional materials? Overview of their properties
- Classes of ultrahigh thermal conductivity materials: monolithic and composite
- Properties of key monolithic carbonaceous materials
- Properties of key metal matrix composites
- Properties of key ceramic matrix composites
- Properties of key carbon matrix composites
- Properties of key polymer matrix composites
- Thermally conductive, low-CTE printed circuit boards
- Manufacturing methods for advanced materials
- Using advanced materials to improve manufacturing yield
- Lessons learned
- Cost considerations
- Applications of ultrahigh-thermal-conductivity-materials
- Future directions, including carbon nanotubes
- Summary and conclusions

Who Should Attend:

Engineers, scientists and managers involved in microelectronics, optoelectronics and MEMS/MOEMS thermal management and packaging design, production and R&D as well as material suppliers should benefit from this class.

3. VERTICAL (3D) HYPER-INTEGRATION AND PACKAGING OF MICRO-NANO-SYSTEMS

Course Leader: James Jian-Qiang Lu – Rensselaer Polytechnic Institute

Course Objectives:

An overview of vertical (3D) hyper-integration and packaging of micro-nano-systems will be presented, including motivation, key technologies and status towards commercialization. The major motivations discussed include miniaturization of micro-systems; performance increase in speed and data bandwidth due to massive small-sized inter-chip interconnects; heterogeneous system integration of variety of technologies; and lower manufacturing cost for specific applications using particular 3D platforms.

In this course, 3D hyper-integration technologies are divided into 4 categories – transistor build-up, wafer-to-wafer stack, die-on-wafer assembly, and packaging-based 3D. In transistor build-up 3D, active devices are built-up over an IC wafer. In wafer-to-wafer stack 3D,

different systems are first fabricated independently and then stacked and interconnected vertically. The die-on-wafer assembly is similar to SoC approach, but with known-good-dies (KGDs) assembled on an IC wafer, then processed in wafer-level. In the last category, the ICs are packaged vertically in die-to-die, system-in-packaging (SiP) and package-on-package (PoP) fashions.

This course will discuss all these technologies, with emphasis on wafer-to-wafer 3D hyper-integration and potential applications. Sample designs and applications towards commercialization will also be presented. The issues associated with each technology category will be discussed, including integration architecture and design tools, yield and cost, thermal and mechanical constraints, and manufacturing infrastructure. Finally, future directions into micro/nano/electro-opto/bio system hyper-integrations including MEMS will be presented, showing 3D hyper-integration as a very promising emerging architecture for future computer, network, nanotech, and biotech.

Course Outline:

- Challenges of current ICs and packaging
- Why 3D Integration?
- Overview of 3D integration and packaging technologies
- Transistor build-up 3D integration
- Wafer-to-wafer stack 3D hyper-integration: Key unit processes;
- Through-Silicon-Vias (TSV);
- Oxide-to-oxide bonding (via-last);
- Dielectric adhesive bonding (via-last);
- Metal-to-metal bonding (via-first);
- Metal/adhesive redistribute
- Die-on-wafer assembly 3D hyper-integration
- Packaging-based 3D hyper-integration
- Technology status, assessment and challenges/issues
- 3D-enabled designs and applications
- 3D Hyper-integration perspectives and technology projections
- Conclusions

Who Should Attend:

Engineers, managers and executives involved in future R&D investments, assembly and product development of electronic packaging, and wanting a fundamental understanding of 3D technologies, as well as the materials and equipment suppliers wanting to know about the existing and future 3D integration technologies and options, will greatly benefit from this course.

4. FROM THICK WAFERS TO THIN CHIPS - CHALLENGES IN PREASSEMBLY

Course Leader: Werner Kröninger – Infineon Technologies

Course Objectives:

This course introduces the technologies and methods used for thinning wafers down to ultra-thin applications. Preassembly is the main enabler for 3D technologies. Thinning and separation of dice will both be covered, especially chip separation has most interesting new developments which will be discussed in detail. Most logic-ICs are going thin for improved heat-dissipation, reduced electrical resistance or improved mechanical flexibility. Preassembly, linking Front-End and Back-End by transferring the wafers into chips, has two main spheres: wafer-thinning and chip-separation. An overview regarding the different process-flows for thinning chips will be given. Emphasis will also be placed on several processes of back side treatment, improving the mechanical performance of the chips. Potentials and opportunities of these process-flows are discussed. Current and future technologies for chip-separation, including all state-of-the-art flows, will be presented. The various separation-processes and their pros and cons will be covered in detail. Emerging technologies will also be discussed and evaluated. The resulting mechanical properties, important for the performance of many devices, will be presented. Topics and solutions regarding the handling of thin wafers and assembly of thin chips will also briefly be covered. This will help potential users to make decisions about the suitability of these technologies for their applications.

Course Outline:

- Applications for thin dice
- Technologies of wafer thinning: grinding, wet-etch, polish, dry-etch
- Inside silicon: the process of Grinding
- wafer bow and wafer warp
- Stability and flexibility
- Back side treatment, chip-thickness and –strength
- Limits to thinning wafers
- Relevant for dicing and packaging: Surface features
- The general influence of dicing in producing chips
- Combination: separating by thinning
- Ways of separating the dice: Current and emerging technologies
- Shipping & handling and assembly of thinned wafers and dice

Who Should Attend:

The course is intended for technical managers in preassembly and aims at fundamental understanding of thinning and singulation processes. It is also very helpful for staff-and management members in making decisions on what processes to use for their applications. Engineers and managers of die-bonding (back-end) and packaging engineers should also attend to see the increasing influence of preassembly to their field.

5. THROUGH SILICON VIAS AND MICROVIAS FOR HIGH DENSITY INTERCONNECTS IN ADVANCED PACKAGES

Course Leader: Ricky Lee – Hong Kong University of Science and Technology

Course Objectives:

Through silicon vias (TSVs) are one of the major enabling technologies for 3D integration and 3D packaging. In recent years, TSVs have attracted substantial attention in the industry and the academia. This course will elaborate on the latest development and the most important research results of forming and plugging TSVs. In addition, the forming and filling of microvias on organic PCB/substrates with build-up layers will be presented as well. The applications of these two levels of high density interconnects (HDIs) in advanced packaging will be introduced. Some related reliability issues will be addressed. For professionals active in microelectronic packaging research and development, this is a timely summary of progress in all aspects of this fascinating field. The lecture contents are based on the instructor's books, his recent research results, and interactions with the packaging and assembly industries. The scope of this course covers overview of HDI technologies, via forming and plugging processes, insulation/barrier/adhesion and build-up layers, characteristics of copper diffusion, various applications and reliability considerations. With the information provided in this lecture, the attendees will acquire a practical understanding in the design, materials, processes, and reliability issues of high density interconnects in advanced packaging.

Course Outline:

- Overview of high density interconnect (HDI) technologies

- Forming of through silicon vias (TSVs)
- Deposition of interfacial multi-layers on the wall of TSVs
- Plugging of TSVs
- Applications of TSVs
- Organic PCB/substrates with sequential build-up layers
- Forming of microvias on organic PCB/substrates
- Filling of microvias
- Special high density interconnect technologies
- Reliability issues of high density interconnects

Who Should Attend:
This short course is intended for research scientists, professional engineers and technical managers who are involved in IC packaging, component assembly, materials and processing, contract manufacturing and marketing.

6. MOISTURE RELATED RELIABILITY IN ELECTRONIC PACKAGING

Course Leader: Xuejun Fan – Lamar University

Course Objectives:
This course will present a state-of-art and in-depth overview of recent advances in moisture related reliability studies in IC packaging. The course provides fundamental knowledge and understandings on the failure mechanisms associated with moisture such as delamination/cracking during reflow, material and interface degradation during HAST, as well as the electrochemical metal migration and corrosion under biased HAST condition. General reliability test practice, qualification, and the different failure mechanisms will be presented. The accelerated test methodology and experimental validations will be discussed. The course will cover moisture diffusion principles and the characterization of moisture related properties, such as diffusivity, solubility, saturated moisture concentration, and the hygroscopic swelling, and adhesion. The vapor pressure evolution at elevated temperature, especially for lead-free applications and reliability concern, will be discussed. The impact of hygroscopic swelling on copper/low K structures as well as under bump metallurgy (UBM) failures will be described. The key challenges in reliability performance for ultra-thin 3-D stack-die chip scale packages and the selection of wafer level film (WLF) will be discussed. The optimization of reflow profile to reduce the failure rate will be introduced. Several case studies related to moisture-induced failures in different types of packages such as flip chip package, TSOP, QFN, and stack-die chip scale packages will be presented. Course Objectives: 1. Fundamental understanding on moisture-induced failure mechanisms under different accelerated testing conditions; 2. Knowledge on material behaviors in the presence of moisture and the impact on reliability performance; 3. Identification of key material properties related to moisture and material selection guidelines; 4. Familiarity of the existing tools to perform the moisture related modeling and material characterization. 5. Case studies for preventing packages from moisture-induced failures such as flip-chip package, QFN package, Stack-die chip scale packages and TSOP packages.
Course Outline:

- Introduction
- Moisture related reliability test and specifications – MSL, HAST, BHAST etc
- Typical failure modes and failure mechanisms in the presence of moisture
- Moisture diffusion – theory and applications
- Moisture absorption vs. water absorption
- Characterization of moisture related material properties
- Vapor pressure evolution at reflow temperature - what's the impact when lead-free soldering is applied?
- Case study – underfil selection in flip chip BGA applications
- Case study – wafer level film failures in 3-D stacked chip scale packages
- Hygroscopic swelling – the impact on low K/Cu interconnect with silicon-package interaction
- Effect of moisture on material properties
- Accelerated test with moisture - can we further accelerate the test?
- Case studies – QFN, TSOP, Flip-Chip

Who Should Attend:
The course is designed for staff members, technical managers, design and manufacturing personnel, and reliability engineers in microelectronic companies. Although the course reviews most recent advances in moisture related reliability issues, the course does not assume prior knowledge of these issues and hence is of interest for both experts and new actors in this area.

7. DEEP SUBMICRON AND NANOSCALE CMOS PROCESS TECHNOLOGIES

Course Leader: Badih El-Kareh – Independent Consultant

Course Objectives:
Dr. Badih El-Kareh will give an overview of CMOS processes associated with today's semiconductor devices. He will cover CMOS components, conventional CMOS technologies, scaling to deep submicron dimensions and enabling processes, scaling limitations, and enhancements for nanoscale generations, including strained silicon, new gate materials, high-K and low-K dielectrics, and three-dimensional structures.
Course Outline:

- CMOS components, silicon crystal
- Junctions and contacts
- MOSFETs, CMOS
- Conventional CMOS, process technologies, silicon crystal
- Insulators, doping and etch techniques
- Contacts and metallization
- An integrated CMOS process
- Scaling to deep submicron
- Why scaling, scaling scenarios
- Enabling process technologies, copper metallization
- Scaling and limitations
- Nanoscale CMOS
- Mobility enhancement techniques, strained silicon
- New gate material, high-K dielectrics
- Low-K inter-level dielectrics
- Three-dimensional structures, outlook

Who Should Attend:
The course is intended for industrial and academic professionals who need an overview of submicron and nanoscale CMOS process technoligies.

8. FUNDAMENTAL AND RECENT ADVANCES ON POLYMERS AND NANO-COMPOSITES IN ELECTRONIC AN

Course Leaders: CP Wong – Georgia Tech;
Ephraim Suhir – Univ of California

Course Objectives:
Describe the application of polymeric materials in electronic, opto-electronic and photonic packaging (underfills, embedded passives, adhesives, encapsulants, insulators, dielectrics, and even conductive elements for interconnects), indicate the major differences in the

requirements for, and applications of, polymeric materials in microelectronic and photonic packaging, elaborate on the potential of nanomaterials and nanotechnologies in electronics and photonics packaging, Material formulators, suppliers and users should have a thorough understanding of the merits and shortcomings of the existing polymeric materials, as well as of the recent advances in the field, and, first of all, in the area of nano materials and technologies, and what has been achieved and could be expected owing to their applications in components, packaging and manufacturing technologies. What You Will Learn: 1. Fundamental and State-of-the-art and challenges in Polymers in electronic and photonic packaging 2. Materials properties, mechanical behavior and reliability of polymer-coated electronics, optical fibers, and role of predictive modeling 3. What is going on with the nanoscale functionalized materials 4. What could be gained by using nanomaterials and nanotechnologies in microelectronics, opto-electronics, and photonics.

Course Outline:

Brief overview of electronics, opto-electronic and photonics packaging : materials, designs, reliability

Polymeric materials in electronic and photonic packaging

Novel No Flow, Advanced and Reworkable Underfills for Flip-chip Applications

Conductive adhesives and nano-lead-free Alloys for lead-free Interconnects-Fundamentals and Recent Advances

Low-cost High Performance Embedded Passives Materials and Processes

Recent Advances on Low Dielectric(k), Nano- functional Materials(high k polymer-composites).

Polymers use in electronics and coated optical fibers

What are nanomaterials and nanotechnologies?

Some rent and future applications of nanotechnology in micro- and opto-electronic packaging and beyond

Who Should Attend:

Engineers, applied scientists and technical managers involved in the design, processing and manufacturing of micro- and opto-electronic materials and systems, in micro- and opto-electronic packaging and reliability evaluations, as well as material suppliers and users should benefit from taking this course.

AFTERNOON COURSES
1:15 - 5:00 PM

9. DESIGN FOR RELIABILITY AND RELIABILITY TESTING OF LEAD-FREE INTERCONNECTS

Course Leader: John Lau – IME

Course Objectives:

In this course, participants will learn the principles of design for reliability (DFR) and reliability testing and data analysis, and lead-free interconnects. Emphasis is placed on the solder-joint reliability of solder-bumped flip-chip assemblies, solder-balled BGA assemblies, solder-bumped fine-pitch CSP and WLCSP assemblies under thermal fatigue, isothermal fatigue, mechanical bending and shearing, and shock & vibration conditions. Also, up-to-date lead-free solder-joint reliability data of high-density PCA are presented.

Most of the materials are based on the instructor's recently published textbooks, "Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies", "Electronics Packaging", "Chip Scale Packages", "Low-Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies", "Microvias for Low-Cost High-Density Interconnects", and "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive Adhesive Materials". (McGraw-Hill publishes all these books.) Each participant will receive a comprehensive set of handout notes.

Course Outline:

Understand all important aspects of BGA, WLCSP, and flip chip technologies

Know the state-of-art of lead-free soldering

Know the effects of X on the IMC and Cu consumption of SnAgCuX solder joints

Material properties of lead-free solders

Know how to do design for reliability (DFR) of lead-free solder joints

Understand the real meaning of reliability

Know how to do reliability testing and data analysis

Know how to determine the true Weibull Slope and true characteristic life

Help your company to make important decisions on lead-free reliability issues

Identify key parameters that impact the solder joint reliability of your products

Avoid potential reliability problems of your high-density lead-free products

Predict reliability, failure rate, and MTTF of your lead-free products

Who Should Attend:

If you are involved with any aspect of the electronics industry, you should attend this course. The content is recommended for component, packaging, design, material, process, equipment, reliability, product assurance, quality control, manufacturing, vendor, marketing, and sales engineers and managers. It is equally suited for R&D engineers and scientists.

10. ON-CHIP THERMAL MANAGEMENT OF NANELECTRONIC COMPONENTS

Course Leader: Avram Bar-Cohen – University of Maryland

Course Objectives:

The rapid migration of microelectronics into nanoelectronics, with the consequent rise in transistor density and switching speed, has led to steep increases in die heat flux and growing concern over the emergence of on-chip "hot spots". In the absence of new and more aggressive thermal management techniques, nanoelectronic chips can be expected to experience accelerated failure rates and an overall loss in IC reliability and performance. The application of on-chip high heat flux cooling techniques provides a most promising direction for the thermal management of nanoelectronic components and is the focus of this Professional Development course.

Successful development of this cooling strategy requires the integration of thermal management principles and concepts into the design and development process from the earliest stages of chip design. Consequently, the course will begin with a brief review of the iNEMI and ITRS thermal roadmaps and a review of the thermal packaging technology options. Attention will then turn to emerging high flux, on-chip cooling techniques, including solid state thermoelectric coolers-both miniaturized and thin-film TEC's, orthotropic spreaders, and dielectric liquid cooling

Course Outline:

Industry Roadmap for IC technology and packaging

iNEMI thermal management Roadmap

Thermal management options – air, liquid, refrigeration

Emerging high heat flux cooling techniques: solid-state refrigeration – miniaturized and thin-film TEC's, dielectric liquid cooling – spray cooling, pool boiling, two-phase microgap coolers.

Wrap up: What have we learned?

Who Should Attend:

This course is aimed at product managers, research staff, and packaging specialists involved in the design, development, optimization, and testing of advanced micro- and nanoelectronic products. Developers of advanced thermal management technology would also greatly benefit from this course.

11. SYSTEM-ON-PACKAGE (SOP) VS. SYSTEM-IN-PACKAGE (SIP), AND SYSTEM-ON-CHIP (SOC) NE

Course Leaders: Rao Tummala and Mahadevan Iyer – Package Research Center

Course Objectives:

This course presents an overview for highly integrated and microminiaturized convergent systems with consumer, computer, communication and bio-medical functions implementing an integrated approach to digital, analog, RF, optical and sensing technologies. The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market IC-package co-design-centric microsystems packaging design and technology flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOP's design flexibility and simplicity, lower cost, and higher electrical performance, and without the intellectual property issues that dominate SOC. To realize these enormous advantages, new SOP sub technology paradigms are required. These include mixed-signal design, ultra high-density embedded digital, embedded optoelectronics and embedded RF component integration as well as wafer level packaging (WLP) and assembly, test and burn-in, thermal management and system reliability. This course makes a compelling case for and presents the status of SOP R&D around the world and compares and contrasts with SOC, SIP and MCM.

Course Outline:

- System trends to convergent micro miniaturized systems
- Semiconductor trends to SOC
- IC and systems packaging evolution
- What is SOP and its Global developments
- SOC, SIP, MCM and SOP – Definitions, Technologies &Applications
- SoP for Digital, RF, Optoelectronic & Sensing Applications
- Technologies & Challenges in SOP Assembly, Thermal Management and Reliability
- Embedded Actives & Passives using SOP Technologies
- Applications of nano materials in SOP
- Convergent Bio SOP Technologies

Who Should Attend:

This course is an overview course and is suitable for all levels of R&D management, senior engineers and executives involved in technical strategy, R&D, design, manufacturing, process and product development of electronic packaging and systems in automotive, consumer, communication, computer, bio-medical, and aerospace industries.

12. WAFER LEVEL – CHIP SCALE PACKAGING

Course Leader: Luu Nguyen – National Semiconductor Corp.

Course Objectives:

Wafer Level-Chip Scale Packaging (WL-CSP) has gained momentum in the small chip arena, driven by needs for cost reduction, form factor shrinkage, and enhanced performance. This course will provide an overview of the WL-CSP technology. The market drivers, benefits, and challenges facing industry-wide adoption will be discussed. The current WL-CSP configurations will be reviewed in terms of their construction, manufacturing process, and published electrical and thermal performance, together with package and board level reliability. Since the technology marks the convergence of fab, assembly, and test, discussion will also address some fundamental issues such as: 1. Does it fit best with front-end or back-end processing?

2. Will it be applicable and cost-effective for memory and other complex devices such as ASICs and microprocessors?

3. Are the current standards for design rules, outline, and reliability applicable? Extensions to higher pin count packages and other arenas such as RF and MEMS will be reviewed.

Course Outline:

- Wafer Level-Chip Scale Packaging (WL-CSP) definition
- Market drivers for WL-CSPs
- Benefits of WL-CSPs
- Barriers and challenges for WL-CSPs
- Review of current WL-CSPs in the industry
- Wafer level testing – status and challenges
- Infrastructure service providers
- Case studies of WL-CSPs (structures, processing, reliability, applications)
- Extension of WL-CSP concept to other arenas (sensors, imaging, MEMS, etc.)
- Future trends: enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra thin WL-CSP, stacked WL-CSP, MCM in "reconstituted wafers," embedded components, etc.)

Who Should Attend:

The course will be useful to the following three groups of engineers and scientists:

1. Newcomers to the field who would like to obtain a general overview of WL-CSP.

2. R&D practitioners who would like to learn new methods for solving CSP problems.

3. Those considering WL-CSP as an alternative for their interconnect systems.

13. EMBEDDED PASSIVE TECHNOLOGY AND COMMERCIALIZATION

Course Leader: Richard Ulrich – University of Arkansas

Course Objectives:

This course will be a comprehensive review of potential applications, commercialized technology, and possible future directions in integrated passive components and processing for organic boards. The organization of the course centers on the benefits and problems with their implementation in order to help potential users make decisions about their applicability in a given situation. Considerable time will also be spent on the candidate materials and processes for integrated resistors, capacitors and inductors in order to help the potential user decide what processes can provide the needed electrical performance while being compatible with their existing substrates and fabrication technology. Emphasis will also be placed on electrical testing, since users of integrated passives will find themselves in the business of producing passive components, not just buying them, and since the electrical performance characteristics of integrated passives can be very different from their surface-mount counterparts, possibly providing significant competitive advantages. Several current potential applications will be described, with particular emphasis on decoupling. The course emphasizes applicability to manufactured microelectronic systems and includes theoretical material necessary to support that purpose.

Course Outline:

- Definitions, Why Use EP's, History
- Substrates of Interest, Thick vs. Thin Film
- Embedded Resistors
- Embedded Capacitors
- Dielectric Choices
- Embedded Inductors
- Electrical Measurement of EP's
- Decoupling
- Filtering
- Termination
- Economic Tradeoffs
- Tolerance, Repeatability and Yield
- Commercialized Systems
- Barriers to Market Penetration
- Where are EP's Going?

Who Should Attend:

Engineers and scientists involved in electronics packaging, circuit board manufacture, electrical design and passive component technologies will benefit from taking this course. The course emphasizes, in order of coverage, motivations for integrated passives, processing, applicability to current systems, materials science, and electrical performance. Anyone in those areas would benefit.

14. ADHESION AND FRACTURE IN MICROELECTRONIC PACKAGING

Course Leader: Mikel Miller – Texas Instruments

Course Objectives:

This short course will explain adhesion, fracture and material concepts as they pertain to microelectronics packaging reliability. Taking a pragmatic rather than esoteric approach, the course is designed to provide a framework for engineers and managers to better understand, solve and potentially avoid adhesion related reliability issues at their respective organizations.

The course will start with an introduction to physical and chemical adhesion, fracture mechanics and material behavior as it pertains to electronic packaging materials. The focus will be to understand what factors play a role in developing interfacial stress and determining interfacial strength. After these fundamentals are discussed, the course will present several adhesion testing techniques germane to microelectronics, discussing what tests are appropriate for each material and the pros and cons of each. This will include interfacial strength testing techniques such as stud pull, button shear and laser spallation and interfacial fracture mechanics techniques such as beam bending tests. Emphasis will be placed on determining which technique is appropriate and feasible for a given situation. Finally, several examples of adhesion related failures in microelectronic components will be discussed and analyzed by applying the earlier learned concepts to each situation. Examples will include issues from flip-chip and leadframe packaging.

Course Outline:

- Adhesion, Fracture and Material Fundamentals
- Chemical Adhesion
- Physical Adhesion
- Fracture Mechanics
- Material Behavior
- Adhesion Measurement Techniques
- Strength of Materials Adhesion Testing
- Fracture Mechanics Adhesion Testing
- Examples of Adhesion-related packaging failures
- Application of adhesion concepts and testing techniques for packaging development

Who Should Attend:

Engineers and technical managers relatively new to thermomechanical reliability of microelectronic packaging, or those wishing to refresh their fundamental understanding of the field will benefit from taking this course.

15. CHALLENGES IN MEMS AND BIO-CHIP PACKAGING

Course Leader: C. S. Premachandran – Institute of Microelectronics

Course Objectives:

Challenges in MEMS and Bio-chip Packaging MEMS is an emerging market in the electronic and medical sector .Many conventional devices are being replaced by silicon based MEMS devices. MEMS devices are manufactured by micromachining silicon for mechanical structures, thin diaphragms, actuators etc. Using silicon process the MEMS devices can be fabricated into tiny chips and is easily integrated into CMOS platform. MEMS devices have wide applications such as mobile phones, hand held devices, automobile, medical products, consumer market etc. So MEMS play a key role in everybody's daily life and has become an indispensable part of the human life.

A final product is realized after packaging the chip. MEMS packaging requires many challenges such as hermetic, vacuum, damping, external access to the media outside etc. Packaging of MEMS device becomes much more challenges than the conventional packaging. To meet the tiny requirement of the package, wafer level packaging, Through silicon via(TSV) ,bumping technologies are aggressively trying to use it to meet the above requirements. Bio chip packaging require more attention than the MEMS packaging because the fluid flow in narrow channels, leakage, evaporation, hydrophobic requirements need to be addressed. Biosensors use MEMS devices to control the body movements, body measurements, imaging etc to understand the body function. Packaging of these devices is a challenge due to the interaction of this packaging with the body.Packaging requirements for implantable chips demands stringent requirements and need to be addressed during the initial product development time.

Course Outline:

- MEMS packaging Introduction
- Wafer to wafer bonding
- Low stress packaging
- Hermetic packaging requirements
- Vaccum packaging requirements and challenges
- wafer level packaging for MEMS
- Microphone, accelorometer, Bolometer ,RF MEMS ,Optical MEMS packaging
- Low temperature wafer-wafer bonding for MEMS
- Biochip packaging requiremnts
- Microfluidic packaging
- Packaging requirement for Lab on a chip(LOC) applicaions
- Thermal considerations for Polymer chain reactions
- Biosensor packaging requirements
- optical Biosensor packaging for bio-imaging
- Implantable sensors
- Reliability requirements

Who Should Attend:

This course is intended for engineers and managers who are involved in the development of MEMS,Bio-chip devices and systems employing sensor,electronic, bio and optical components. This course aims to give an overview and basic packaging requirements on rapidly developing new areas on bio-packaging and mems packaging.

16. TRENDS IN 3D PACKAGING

Course Leaders: Jan Vardaman – TechSearch International, Inc; Phil Garou – TechSerach International, Inc

Course Objectives:

3D packaging is the answer for space constrained applications and products that require greater functionality in a smaller space. 3D packaging offers improved performance for a variety of applications ranging from portable products to space. 3D packaging includes stacked die as well as package on package (PoP) configurations.

Through-hole silicon via (TSV) is the ultimate 3D interconnect. Driven by the need for improved performance and the reduction of timing delays, methods to use short vertical interconnects have been developed to replace the long interconnects found in 2D structures. The industry is moving past the feasibility (R&D) phase for TSV technology into the commercialization phase where economic realities will determine which technologies are adopted.

3D integration with through silicon vias (TSV) includes:

- Through wafer via technologies
- Thinning of wafers
- Wafer-to-wafer and die-to-wafer bonding

This tutorial focuses on the developed of 3D packaging and the current high volume production parts. The tutorial also covers the key enabling technologies for through silicon via formation. Various methods to fabricate vias are described. Enabling unit operations are discussed including:

Course Outline:

- Development of 3D packaging and the current high volume production parts
- Key enabling technologies for through silicon via formation
- Methods to fabricate vias
- Enabling unit operations
- Critical factors limiting the adoption of TSV technology

Who Should Attend:

Packaging engineers that are space constrained in their designs will find the answers that they are seeking by taking this tutorial.

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IEEE CPMT Society Newsletter

Send inputs, suggestions, and articles by email to nsltr-input@cpmt.org

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