ing in guest editors from the wilds and then after trial by fire making them associate editors.

In these new times of mostly electronic (not paper) transactions it is no longer clear that 3 Transactions are needed to cover the breadth of CPMT. One no longer worries so much about a thick publication or not being able to find papers of interest to you in a huge table of contents.

Timeliness goals: in looking at papers over 2 years, more than 80% must have been published in less than 12 months. In addition, 50% of submittals must have the first decision (reject or edit) occur within 120 days. For the last year we have had an IEEE staff expert help us monitor the paper flow and push the 113 delinquent papers through the system. Only 17 papers remain in the system that started before 2006.

A workshop to help authors is being offered at some of our conferences. This "Best Practices" workshop was offered at ECTC and attracted about 30 attendees. The newsletter will be expanded to include technical papers and perhaps so advertising of interest to members.

Wayne proposed the Society support a part-time publication expert to work on the newsletter expansion, laggard Transactions papers, and provide communication amongst volunteers. Resolution passed.

Conferences:
Rolf Aschenbrenner, VP Conferences, summarized that CPMT held 26 meeting this year compared to 30 last year. The Polytronic and Portable conferences decided to merge and will meet in Garnisch-Partenkirchen Germany in August.

The ESTC 2008 will be in September in Greenwich, Britain with 270 papers and 16 special presentations.

Phil Garrou and Paul Franzon proposed a new 3-D Silicon international workshop for April 2009. This workshop may rotate to Europe, Asia, and North America. The scope of the meeting is still flexible. The Board approved this initiative.

Technical Committee:
Rao Bonda, Technical VP, reviewed the status and web pages of the various technical Committees. He pointed out that TC-12 has modernized their web presence and is working with all the other committees with this goal. TC-11 has a new title – Electrical Test – Semiconductor Wafer and Packaging.

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IEEE CPMT Society Field Award for 2008

Submitted by Dr. Leonard Schaper, Board of Governors – Member at Large, IEEE CPMT Society

The 2008 IEEE CPMT Field Award was presented on May 29, 2008, at the ECTC Conference in Orlando, Florida. The 2008 award was given to:

KARL PUTTLITZ SR. (F'IEEE) - President, Puttlitz Engineering Consultancy, Wappingers Falls, NY USA; and
PAUL A. TOTTA – (non-member) Retired, IBM East Fishkill Facility, East Fishkill, NY, USA,

"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages"

Karl Puttlitz and Paul Totta were part of a small development team at IBM in the early 1960s that initiated the development of the flip-chip interconnection. They established this new interconnection technology in the IBM System 360 computer line. While it has remained the primary interconnection method for IBM, these packaging technologies are found around the world in handheld products, i.e. cell phones, in advanced computer systems from laptop machines to mainframes, and in a wide variety of telecommunication equipment. Flip chip technology developed by this team is now practiced throughout the industry and has been an enabler for advanced systems and miniaturization of electronic packages and handheld systems.

Paul worked on the device side or the interconnection in an effort called Solid Logic Technology (SLT). Key to the advancement of the technology was the concept of using glass passivation on silicon devices. The glass film avoided corrosion and degradation of the device and freed the package from hermetic encapsulations which were expensive and not so reliable. As a young metallurgist entering electronics for the first time, he co-invented the concept and process for creating a metallization pad through the glass, evaporating high-Pb solder and using "homemade" copper balls as contacts and connections between the silicon device and its hybrid, thick film package. The cost of chips was reduced by orders of magnitude and the vibratory-bowl random handling of chips facilitated highly productive, low cost manufacturing. The attached chips were much more rugged and reliable than the hermetically sealed, wire bonded counterparts.

Karl worked on solder-dam development post-fired, glass thick films deposited near the ends of conductor lines forming pads to which the chip solder bumps were reflowed. The dams prevented the molten solder from running down the conductor lines during chip reflow, i.e. prevents solder joint collapse – hence the term "controlled collapse chip connection" or more popularly, C4 joint.

The early ceramic circuit boards required thick-film technology and integrated circuit elements which would be a compatible platform for the C4 devices. Karl developed both the thick-film technology used by IBM and formulations used for its integrated circuits printed on ceramic chip carriers: conductor lines, resistors, capacitors, inductors, humistors, and thermistors.

Thus, IBM's System 360 computer line was very successful because of these packaging and interconnection innovations as well as the system concepts. However, the interconnection system required many innovations on both the device side and carrier

side. As a team, Paul and Karl worked the system out using some of the examples of technology developments below.

Paul's metallurgy background led him to approach problems with semiconductors differently than the EEs and physicists who were on the multidisciplinary team. For instance, the solid-state alloying at the AI contacts, the "penetration problem," was relatively easy for him to understand and explain. It was initially fixed by "doping" AI with Si to satisfy the solid solubility of Si into Al during thermal processing.

As IBM evolved the chip technology from single, discrete devices to integrated circuits, new problems were discovered in the thin film wiring such as electromigration opens of the wires. This problem was solved by colleagues who invented copper doping of the AI. This added orders of magnitude to the current-carrying lifetime of the chip wiring. But then, the Cu-doped AI began disappearing during processing in the line. It was his privilege to determine that the "missing AI" in the line was actually a corrosion phenomenon. The solution to the problem essentially stopped the manufacturing impasse and got him a contribution award as well as reputation of "chief troubleshooter." About this time he was invited to manage the Device Metallurgy Department in the laboratory. One of his first efforts was to replace the AI on AICu-based chip wiring with Ag and Cu wiring. This high conductivity chip wiring was not only more conductive, but more electromigration-resistant as well. IBM's first patent featuring Cu wiring was a Totta/Mutter patent of 1970. Flip chip core drivers were actually made and shipped with this technology, clearly a forerunner of what was to come in the 1990s.

By 1972 Paul took responsibility for chip passivation, and then RF sputtered SiO_2, and multilevel wiring of chips. This included solving via hole problems, planarization techniques and reliability issues. Along with multilayering came the opportunity for "area array". The bump counts rose to about 100 C4s. When flip chips on the alumina substrate grew in size, the low cycle thermal fatigue of the solder became an issue. One of his departments spent much effort in understanding solder fatigue and fracture. This led to shape factors, alloy changes (e.g. Pb In), and other things to extend lifetime.

In the 1970's IBM devised multilayer ceramic (MLC) chip carriers capable of wiring out flip chips with a full array of I/O solder bumps. The chips are directly reflowed to micro sockets formed by co-fired molybdenum vias that intersect the surface, and plated with electroless nickel to render them solderable. However, the electroless nickel, plated from a hypophosphite-based bath, exhibited several unacceptable conditions resulting from phosphorous entrained in the nickel deposits. Cracks occurred due to high internal stresses created; and worse, a nickel phosphide (Ni3P) layer, not wet by solder formed at the solderlmicrosocket interface. This layer caused some solder joints to separate at that interface as identified in Karl's award-winning 1990 IEEE Transaction paper.

His work defined the need for change and he helped provide the innovation with his co-invention of an electroless cobalt plating bath. It demonstrated the feasibility of utilizing an organic boride reducing agent (DMAB), in place of the hypophosphite. Henceforth, a nickel bath was formulated based on DMAB, similar to the cobalt bath. The DMAB-based nickel bath was successfully utilized for several decades for all of IBM's MLC flip chip products.

Karl played a major role in the invention of a method to salvage electrically-good flip-chip devices by restoring the solder bump array subsequent to a reflow attachment and removal from a chip carrier. This was a significant innovation, since electrically-good devices are very scarce in the early development stages of a device program.

Chip replacement capability was a key to IBM's strategy of using highly populated (with 9 to 133 chips) multichip modules (MCMs) for its mainframe computer CPUs. This required the capability to replace one or more chips on these MCMs in order for the computer programs to be economically viable. Replacement allowed meeting yield targets and field upgrades with enhanced chip sets. Karl provided the solution by leading a small development team that invented the flip chip replacement tooling and processes that IBM utilized in its manufacturing plants worldwide for more than 25 years starting in the late 1970s

Replacement consisted of a variety of technologies (e.g. mechanical, ultrasonic, hot gas and infra red heating that allowed individual flip chips to be removed from a closely-spaced array of chips mounted on a MLC MCM, to dress the solder at the removal site, and then, either locally or globally, reflow a replacement chip. These operations were achieved without physical damage or an adverse reliability impact on the replacement chip, neighboring chips, nor the chip carrier.

As a natural result of their collaboration, Paul and Karl co-edited and co-authored a handbook that covers all aspects of area-array interconnects at both the first and second levels of assembly.

Subsequently Paul and Karl worked to continually improve the materials, processes and reliability of the flip chip interconnections system as noted below.

Paul was appointed an IBM Fellow in 1987 in recognition of his many activities in chip and package interconnection technology. The position gave him the freedom to reinvent the C4 process from a metal mask evaporation process to a sputtered seed layer/plating process. The timely reinvention allowed IBM to continue using C4 interconnection because the old process was not extendable to 300mm wafers and fine pitch bumps with counts of up to 10,000 per chip.

All during Paul's time with IBM, from 1971 until retirement, he participated in ECC and ECTC symposia activities. He was a speaker, often session chair, head of interconnections and short course teacher. It was always a rich and rewarding experience. Since retirement from IBM in 1999, he has been invited back to their Corporate Technical Recognition Event three times for recognition:

1. Outstanding Contribution Award for the reinvention of C4 process in the 90s. (2001)

2. A Patent Portfolio Award for multilayered semiconductor wiring which was sputtered and RIE etched; later used extensively throughout the semiconductor world. (2003)

3. A Patent Portfolio Award for a tungsten contact stud structure and process also extensively used by IBM and the world. (2005)

Karl went on to devote his career in providing sustained technical innovations and technical leadership that greatly contributed to the success of this unique interconnection scheme and other packaging innovations. Karl is recognized throughout the world as a lending expert in microelectronic packaging, and particularly for his contributions to area array technology at both the first (chip-to-carrier) and second (carrier-to-card) levels of packaging.

Karl's technical contributions and leadership are widely recognized. IBM honored him with a Corporate Outstanding Innovation Award, and was elected a Fellow of the American Society of Materials (ASM) International and also an IEEE Fellow "-- for developments and leadership in the microelectronic packaging sciences, particularly area array interconnection technology."

Other Achievements: Karl has made numerous contributions to second level (component-to-board) interconnection technology as well, a few examples are noted.

1. CBGA Dual Solder System: Karl led the effort to define and optimize IBM's dual solder system used for ceramic ball grid array components whose fixed standoff height provides greatly enhanced reliability.

2. Replacement of Components Mounted on PCBs: Karl was a key participant in defining a method and tooling to locally remove surface mount (SM) components like CBGAs from even very thin printed circuit boards (PCBs) and locally reflow replacement components.

3. Rework CBGA/CCGA Components: Karl led a team that defined the method and tooling to rework both CBGA and CCGA components allowing one or more balls/columns to be replaced to enhance yields and reduce costs.

4. National Test Specification: Co-authored "The Production Ball Grid Array (BGA) Socket Test Specification," adopted as a national standard by the Electronics Industries Association (EIA): IS- 701, 7/96. Co-author: T. Peel, Contech Research, Inc.

5. Lead-free Technology: Karl had corporate responsibility working with all aspects of the business (development, purchasing, manufacturing, marketing, quality, legal, etc.) for compliance of all IBM products worldwide with Pb-free legislation. He initiated the program at IBM in 1999 and served as Corporate Program Manager until his retirement in 2004. He played a major role in obtaining flip chip and other exemptions from the European Union Commission favorable to the industry. He is the co-editor/co-author of a lead-free handbook, and actively involved in Pb-free solder joint development.

In summary, Paul and Karl made many vital and sustained contributions in advancing the state-of-the-art of flip chip technology in its infancy. They by necessity worked as a very successful team to develop complimentary thin film and thick film technology to make the C4 interconnection system successful for IBM. Now this technology in the form of flip chip interconnection has spread throughout the industry and remains a major driver and enabler for new products and packages around the world.

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Call for Candidates

Submitted by Ms. Marsha Tickman, Executive Director, IEEE CPMT Society

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of this Newsletter for details.)

Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways: either by the Society Nominating Committee, or by petition.

This year's election is the fourth in which members-at-large will be elected to achieve totals proportionate to the geographic distribution of CPMT members. Voting members will elect members-at-large from within their Region only (that is, members in Region 8 will vote for members-at-large from Region 8, etc.)

Elected Members of the Board of Governors must be willing to attend two annual Board meetings and participate actively in areas of their interest (publications, conferences, membership development, chapter development, etc.) The term of office for this election is 1 January 2009 through 31 December 2011.

If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can become a candidate via petition by following the procedures below.

- Prepare a petition that contains your name, member number, and statement of your qualifications for office.
- Provide lines for signatories. Each line should include space for a printed name, member number, and signature.
- Have the petition signed by a MINIMUM of 46 CPMT Society members in good standing (Student grade members are not eligble to sign.)
- Submit your petition by mail no later than Friday, 25 July 2008 to:

CPMT Society Nominations Committee
c/o Marsha Tickman
IEEE CPMT Society Executive Office
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331 USA

OR

- Request establishment of electronic petition process, allowing signatures to be collected on-line.

You must contact Marsha Tickman to implement electronic petition process.

Membership status of all signatories will be validated. It is suggested that you gather more than 46 signatures in order to assure meeting the minimum required number of valid signatures.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at m.tickman@ieee.org.

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