Mr. Alexandru Borcea was present at every edition of the contest and mentioned that TIE aligns the universities and the business domain, assuring the competitivity of the industry. The diploma received at the end of the contest is on its way to become a certificate.

This year featured new events on the contest schedule: two workshops based on *Traceability in Electronic Packaging and the Nowadays Solutions for Electronic Modules Development.*

For the participants, and especially for the winners, it is a good occasion to keep in touch with trends and a way to get informed about their future career. Students can now decide if what they learn is what companies ask for.

The first Workshop, presented by Mr   Traian Cuhu, Key Account & Distribution Manager Romania & Bulgaria, at Brady Corporation, having as moderator Mr. Alexandru Borcea, had as topics "*Traceability, an Important Key in Electronic Manufacturing*" and draws the steps to follow in manufacturing a ticket for a big variety of products.
The term "traceability" means the steps one should follow in manufacturing the product. Prof. Paul Svasta stated that "a company cannot exist without traceability".

The second Workshop, presented by Radu Serban Ionescu, Ph.D., from the RadioConsult Company and chaired by Prof. Mariana Jurian, Ph. D., had as topic: "*Nowadays Solutions in Electronic Modules Design*".

Dr. Ionescu discussed the problem of planning and manufacturing the components used to create the radio equipment defined through a program or virtually (Software Radio). His presentation ended with an invitation made to the universities who want to improve their lectures and lab platforms to have access at additional material.

And of course, a contest couldn't be without participants and subjects.

The Technical Committee, chaired by Associate Professor Norocel Dragos Codreanu of Politehnica University of Bucharest, was deeply involved in development of the subject for the contest. The developing team gathered teaching staff from each participant university as well the previous winner of the contest, Cosmin Andrei Tamas. As a new comer, Associated Professor Gheorghe Pana Ph.D. from Brasov told us how important the direct involvement in the contest topics development was for him, saying he had a lot to learn from it.

From our SBC there were four participants, one of them (Radu Foti Coleca-SBC Vice-Chairman) obtaining a good result in the final.

The winners of TIE 2008 are students at "Politehnica" University of Timisoara from Professor Horia Carstea, and Assistant Professor Marius Rangu.

Students found the contest a little bit hard, but challenging, and await with great interest next year's edition, which will take place in Galati, hosted by the "Dunarea de Jos" University of Galati, as well as the new ideas (and opportunities) it will bring.

From right to left: Adam Gina, Valentin Nita, Leonard Teasca and Radu Foti Coleca from Politehnica University of Bucharest

The winners of the TIE 2008 contest - From left to right: Trifan Alexandru (third place) Osan Adrian (first place) and Negrea Catalin (second place)

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Conference Reviews:

58th Electronic Components and Technology Conference (ECTC) Update
Submitted by Dr. Dave Palmer, Contributor,
IEEE CPMT Society Newsletter

Luncheon Speaker:

Title: The Global Semiconductor Industry Outlook

George M. Scalise, president of the Semiconductor Industry Association, gave the luncheon presentation at this year's ECTC. He used as his theme "creative destruction," a concept from the works of Joseph Schumpeter. As an example, he pointed out that the transistor vastly improved electronics performance over tubes yet none of the successful tube companies made it big in transistors or ICs. He similarly sees the end of the CMOS era in about 10 years with some yet to be defined Nanotechnology taking over. How can a company make the creative leap without the concomitant destruction?

He pointed out that during such a transition it will be necessary to:
- Commit to IP protection amongst the players
- Compete for investment funds

- Rebuild the development and manufacturing infrastructure

He observed that unlike the days of Bell Labs, all research is now conducted in universities. He further observed that education of students from first grade through the universities will have to continue changing with the changing technology and talent needs, and also that the big 'creative destruction' will require wise tax policies for both research and infrastructure changes.

He has been somewhat disappointed that Washington DC has been mostly talk and little action on these issues, but did point out that some countries are taking the lead (Ireland, China, Singapore, and Israel).

The industry is seeing an 8% growth this year. Memory chips are under severe cost pressure. The PC market is still the number one driver at 40% with the cell phones second with 20%. Other consumer products are at 17%. The industry has grown from $40B in 1995 to $400B soon.

Panel Sessions at 58th ECTC:

3D- TSV Packaging Application – Implementation:
On Tuesday evening at this year's ECTC *William Chen*, President of the CPMT Society, moderated the ECTC Panel Discussion focused on TSV (Through Silicon Vias). About 230 conference attendees skipped Disney World to learn and ask many questions.

Peter Ramm of Fraunhofer IZM discussed the advantage of 3-D systems to provide heterogeneous systems. He used as an example the European e-CUBES project focused on self organizing networks of wireless sensors. Infineon Automotive has created a tire pressure measurement system as a 0.3" cube by combining a 'large' MEMs pressure diaphragm with an RF transceiver and antenna. The system used stud bumps as well as hollow vias to connect layers. His advice was "don't use a complex interconnect for all interfaces but use the easiest technology for each layer." Via metal filling is the most expensive step in TSV at $109; the complete TSV is estimated at $400/wafer. Any of the 3-D solutions often answer the challenge of performance draining interconnection in a 2-D design.

Bob Sankman of Intel emphasized the shorter connection lengths of 3-D allowing a high rate of data communication. This would be particularly helpful with memory stacked on a processor chip, or perhaps a multi-sensor chip on a processor or wireless transceiver. In general where the form factor is the most important marketing need, 3-D should be used. Since TSV is a most complex way to stack layers it should only be suggested for the right market. Bob Sankman suggested that the via last approach is more flexible in manufacture. As to whether you should do wafer stacking or die stacking depends on the application and unit volume. Intel will not go to TSV until they "have to".

Hirofumi Nakajima of NEC Electronics Company mentioned that Japan has been working on TSV intensively since 1990. They use Cu, W, and poly-Si to fill the vias, but contamination must be monitored with copper. Tungsten has lower resistance and finer pitch than poly-Si. They have found chip to wafer bonding as the most cost effective approach for their applications. He showed an image sensor as an example resulting in 0.64 mm package heights. Their target is to perform TSV at $200/wafer. Sony is using face-to-face with 25 micron pitch. He agreed that you need a significant form factor or performance advantage to compensate for the extra cost of TSV. This suggests that a break-through is needed in TSV processes.

Tom Gregorich of Qualcomm says that it is time for each company to either ante-up for TSV or to pass. Qualcomm motivation for TSV process is to include more consumer functions in the same form factors of today's slim units. Unfortunately the consumer judges the product by cost and form factor and performance. The wide ranges of technology in the cell phones make it hard to put everything into one package. The question they ask regularly is "what is next in cell phone packaging." With TSV one must also ask who performs the extra steps, the wafer fab or the assembly line. Tom predicts that TSV will keep improving every year just like wire bonding has just kept going.

Under questioning the panel stated that design for TSV is behind the fab process at this time. There are rules of thumb for TSV design but no automated computer tools. In conclusion, it appears that TSV is something everyone is getting familiar with just in case one more manufacturing breakthrough occurs.

ECTC Panel – Product Development in the Semiconductor Industry:
Senol Pekin, Intel, chaired a packed evening session on Wednesday at the just completed ECTC in May. The perspective for the discussion was set.

- Originator company of new tech bears most of the cost
- Copy-cat companies get higher profits initially
- Profit margins decrease in time

Lesson learned: one needs a series of great ideas to sustain a company. Examples used include Disney domination of animation in the 20s and 30s only to have other companies originate super-hero cartoons and expand the pie of acceptability. Senol Pekin also pointed out that the nylon industry often threatened to stop growing but new markets kept being discovered. The Semiconductor industry is $250B/year today, how will it keep growing?

Jerry Bautista of Intel insisted that an increase of digital power in an IC will continue to double every two years. However, the advance will not depend on diminishing feature size or higher clock rate as much as by architecture such as multicore, and high bandwidth connections to memory and between cores. Application trends will continue to see data bases get more massive: from the 3-D and video streaming of today to some complex sensing and perception applications in the future, e. g. virtual surgery.

Philip Damberg of Tessera discussed how IP based companies can keep growing using Tessera's history to prove his point. Growth comes from anticipating trends before large companies, and buying up small companies that are headed in the right direction.

Hamza Yilmaz of Alpha and Omega enumerated the steps for successful product development and then suggested general rules of thumb.

- Examine new concept and market
- Define initial spec and flesh out justification for investment

- Detailed design resulting in full specification – start system level evaluation
- Customer sampling – system characterization
- Release to manufacture

Success of a Technology company depends on having many products in the development pipeline. Must maintain a process R&D effort separate from specific product R&D or your strength will ebb. When a crisis develops it is important to immediately dig for the root cause reason and not play palace politics. Hamza Yilmaz suggested that we should now use the many computer simulation tools that exist for each step of development.

Ken Williams of Applied Materials explained that every step in the product development pipe sees a reduction of options by 10, thus develop something with lots of options in the design stage. He suggested that the low-K quest has been delayed by 7 years because the initial scope of the development had too few options. He sees "solid state drives" as a new inflection point. If the trends continue 7 new fabs will be needed just to make enough flash memory. The cost of these memories must drop (do we have any technology options lefts?), we need 32nm litho but it doesn't exist realistically in the pipeline (Intel cancelled the Extreme UV litho effort because it couldn't keep on schedule).

Raj Masters of Advanced Micro Devices discussed efficient product development. He added a new rule of thumb – "never have more than 100 check points / milestones on even the most complex project or you will never finish." He suggested it is most important in the production facilities to carefully separate value added steps from waste steps. Some waste steps may be mandated for historic reasons but many can be designed out of the flow. He mentioned that when he enters a plant announcing that he is there to make them "lean" that most engineers mumble "leave us alone, we know what we are doing," but by the time the process is over everyone is lean and mean.

In response to audience questions the following consensus was projected. It doesn't make sense to go to 450mm at this point since there are still other ways to get more ICs out of existing wafers. Companies can grow revenue by going into related markets that benefit from their strengths – ICs to large panel displays to solar cell panels was an example. (so companies can grow fast even if the IC business does not). They predicted the semiconductor industry would continue to grow faster than the world economy. Most were lukewarm toward stacking chips using TSV but they all are developing the technology in case there is a more prime time. Intel may have been bluffing, but suggested that the need to marry external memory at high bandwidth to processors may push TSV for them.

Advanced Embedded Passive and Active Device Technologies:
On Thursday evening of ECTC *Yoshitaka Fukuoka* of Weisti led the CPMT Seminar on embedded components.

Osamu Nakao of Fujikura entitled his presentation "IC Chip-Embedded Polyimide Multi-layer Circuit Board." The original motivation was to make flexible and foldable multi-layer polyimide circuit boards with embedded chips. This approach gave higher density, easier handling, high performance, good reliability, allowed surface mounting if needed, and could conform to system package. The IC interconnections are formed on some foundation polyimide layers to which the ICs are mounted face-down. Face up can also occur but requires vias to be accurately placed in a polyimide layer. It is sometimes necessary to reposition the pads on an IC from dense edge pads to less dense area distributed pads using wafer steps. A pitch of 300 microns is reasonable, allowing a 8x8mm chip to have 600 I/O. The silicon die are typically thinned to 80-100 microns before embedding. Conductive paste has been used to fill vias in polyimide. Particle size is 5-10 microns.

Atsushi Kobayashi of Dai Nippon Printing discussed "The superiority of Buried Bump Interconnection Technology in EPD & EAD PCB manufacturing. The standard BBit process uses 180 micron bump spacing, the advanced is at 130 microns, and the super to be released in one year will be at 80 microns. The embedding is in 6-8 layers with bumps on Cu foil layered with Prepreg. The embedding of components results in shorter interconnect lines and lower cross talk and noise pickup. Bumps are made with screen printing of custom Ag paste. An example was a wrist watch with memory chip. 10 million unit are made a month with 95% yield using Know Good Die.

Yasuhiro Sugaya of Panasonic Electronic Devices presented "Embedded Capacitor Interposer by using SIMPACT. The goals for their embedding were (1) a multi-functional terminal that was smaller but fully functional, and (2) a high speed CPU package with low ESR and ESL. A new paste was develop to act like a via post when attaching the components. Module size reduction was 45 – 60 %. One particular advantage was to bring the bypass capacitors to be right beneath the LSI chip rather than having surface mount caps on other side of mother board. The embedded capacitor sheet is only 100 microns thick instead of the original discrete 1.8mm thickness. A clock rate of 400 MHz was achieved with much reduced power usage. Clock jitter went from 133 to 65 psec.

Akinobu Shibuya of NEC focused on "Si Interposer Integrated with SrTiO3 thing Film Decoupling Capacitors and TSVs." He pointed out that as the speed of ICs keeps increasing, the capacitors must get faster and larger. A goal of one microfarad with short leads is set for any technology. They place a thin film capacitor between the IC and the package/board. The capacitor and the needed interconnections becomes the silicon interposer. An STO sputtered thin film is used to get a dielectric of over 100. This capacitance layer is carpeted everywhere and then patterned so through vias can be made. An IR laser beam is used to find weak points in the capacitor by noticing the increase in leakage due to local heating. Hillocks often correspond to leakage points. They discovered if the film deposition takes place at less than 400 C then no hillocks form. The through silicon vias are 50 micron thick with smooth side walls. Copper is the fill leaving a pad on the top of the via. The STO capacitor wafer is married to the LSI wafer and then dicing is one. Capacitance range depends partly on LSI size and has been 1-7 microfarad.

Ichiro Koiwa of Kanto Gakuim University discussed "Fabrication and Embedding the Thin Film Capacitor Array Prepared by Semiconductor Technology." The driving need is that there was no surface area for capacitors so they had to be embedded. He discussed two dielectric types. One gives large area capacitors with

medium loss: dielectric = 51, delta = .03, Ba0.6Sr0.4TiO3. the second gives medium capacitors and at low loss: dielectric =350, delta = .001, Sr0.9Bi2.1 Ta2.0O9. Platinum films were used as the plates. A master pattern of capacitor sizes was used so that any particular value can be reached by connecting the correct plates. These designs self resonate at 10 GHz for the 65 pF size. There is only a 1% change from 25-150 C. The low K capacitors survive soldering steps on the board.

Many different embedding technologies are being actively used in commercial product manufacturing.

Presentations at 58th ECTC:

Since many Society members were unable to make the ECTC in May a brief summary of some of the talks are below so you can consider ordering a Proceedings CD or search Xplore for more of the presentations.

Session 4 RF components:
1. Sandia Labs describe 3 components developed to allow a portable real-time spectrum analyzer: SiGe RF power divider, monolithic frequency stepped SAW filter, and integrated RF detectors.
2. Sasumu Obata of Toshiba discussed the use of low outgassing polymer used to make adjustable capacitors "hermetic" with wafer processing.
3. Geert Carchon of IMEC described post processing of state-of-the-art CMOS wafers with BCB and Copper to make high Q inductors for high frequency circuits.
4. Emile Davies-Venn of Intel described in detail the circuit design and FCBGA processing to achieve Q~30 for capacitors and inductors used on a WiFi Balun.
5. David Chung of Georgia Tech describes an antenna module for 14 GHz satellite use that can be stacked like LEGOS TM. Liquid Crystal Polymer was the material used.
6. Lianjun Liu of Freescale Semiconductors gave an expansive talk on RF MEMS switch designed for many cycles and low price. The goal is to integrate the switches into a cell phone module so a minimum of components can serve the many bands a phone must respond to.
7. Guoan Wang of IBM discussed board patterning techniques to produce slow wave behavior of 60 GHz circuits. This will allow compact components.

Session 10 Nanotechnology:
1. Yang Chai of Hong Kong University of Science and technology presented development using carbon nanotubes to minimize electromigration of Cu lines on ICs. The resistivity increased by 14% when tubes are include in the electroplating solution. However the electromigration is suppressed.
2. Wei Lin of Georgia Tech described taking aligned nanotubes carpets grown at high temperature but then transferred at low temperature to an assembly. The presentation included a movie showing transfer in an SEM.
3. Jin-Chen Chiu of National Sun Yat-Sen University discussed making a liquid of nanotubes in a polyimide matrix using an ionic liquid to keep the tubes from clumping. This material is applied as EM shielding on a module.
4. Po-Chun Huang of National Tsing Hua University produced nano particles of Tin by evaporating into a gas and used metal salt in liquid to prevent aggregation and oxidation. This paste could fill micro vias on the smallest scale.

5. Trang T. Thai of Georgia Tech described wireless sensors based on nanotubes. This is a simulation study aimed at using them as gas sensors in composites or structures.
6. Shin-Bok Lee of Seoul National University proposed Pd-Ag dendrites at hydrogen sensors. These filaments are more stable than a thin film of Pd which is the current technology.
7. Rabindra Das of Endicott Interconnect Technologies used a raster laser to process dielectric films to make adjustable capacitors. Also, deep channel etching to allow x10 density capacitors was presented.

Session 16 Integrated Passives:
1. Arun Chandra Kundu of Intel compared passives for silicon, glass, and LTCC for a wireless module. All were suitable for production with LTCC being thicker and more expensive and glass allowing smallest form factor.
2. P. Markondey Raj of Georgia Tech discussed dielectric films that give TCC< 30 ppm. They developed low temperature ways to get the right crystal structure from BaTaZno3 and CuZrO3 films.
3. Li Li of Freescale Semiconductor discussed a trade-off study of technology for making Baluns. After succeeding with GaAs they wanted to lower costs by using high resistivity Si wafers.
4. Don Won Lee of Stanford University presented methods to make solenoid inductors with magnetic cores using IC processing. An amorphous CoTaZr film was used as the core.
5. Clemens Ruppel of EPCS AG discussed the high Q filters needed to provide a 55 dB duplexer for cell phones to isolate transmitter from receiver. SAW and BAW devices still win in design and expense over MEMs type designs.
6. Goerge Ponchek of NASA discussed resistors embedded in a Liquid Crystal Polymer. The study characterized the resistors to determine the highest power for which they remain reliable.
7. Kai Liu of STATS ChipPAC compared many substrates for filter and Balun construction. They chose a silicon substrate using IPD technology and made it x6 smaller area and x10 volume. Qualification was performed.

Mahadevan Iyer and Amit Agrawal prepare before the breakfast meeting begins

Electronic Components & RF Committee meeting:

Mahadevan Iyer of Infineon chaired a Friday 7am breakfast meeting for the Electronic Components & RF committee at ECTC. Fourteen conference attendees showed up in addition to two persons calling in. Mahadevan reported that 54 abstracts were received with the right technology focus. Of these 42 were submitted directly to the committee and 18 papers scheduled for presen-

tation. This represented 2.5 sessions at the conference plus one of the evening panels which was completely dedicated to embedded components.

Len Shaper suggested that we include in our next request for papers a focus on high speed digital components (terminations and decoupling caps) and stress was added for papers on wireless sensors. Variations on the committee name were considered to make sure RF and Components were both recognized; the leading contender is "electronic components and RF technology." New names of stakeholders were gathered for next year's e-mailing request. There was a suggestion to mine the names of all authors of papers and presentations of RF and component papers.

Amit Agrawal of Cisco was voted the new chair of the committee. If you want to help grow these technical topics for ECTC and for the CPMT Society contact Amit at ap_agrawal@yahoo.com

Part of committee preparing for next year's ECTC abstract hunt
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2nd International Workshop on 3D System Integration

Submitted by Rolf Aschenbrenner, VP Conferences,
IEEE CPMT Society

The 2nd International Workshop on 3D System Integration took place on 1-2 October 2007 at the Fraunhofer-Society, Munich, co-organized by IEEE CPMT. More than 90 engineers, scientists and entrepreneurs attended the 2-days workshop and discussed about world-wide R&D activities, perspectives and challenges of 3D integration.

After the welcome and introduction by Peter Ramm, Fraunhofer Munich, the keynote address was given by Sitaram Arkalgud, director of SEMATECH (US), on "Paving the Roadmap for Through Silicon Vias". The first day continued focussing on Si-based technologies for 3D IC integration with excellent talks of speakers from ZyCube (Japan), STMicroelectronics (Italy) , EPFL (Switzerland), NXP (Netherlands), SINTEF (Norway), Semitool (US), IBM (Switzerland), CEA-Leti (France) and Fraunhofer IZM (Munich). After the opening talk of Robert Darveaux, Amkor (US), on "Developments of 3D Packaging" the second day´s talks were given by speakers from AT&S (Austria), Techlead (US), Imbera (Finalnd), ASE (US), IMEC (Bel-

gium), Schweizer Electronic (Switzerland), Panasonic (Japan) and Fraunhofer IZM (Berlin).

Speakers and chairs at the IEEE Workshop on 3D System Integration Munich 2007 (sitting right: Keynote speaker Dr. Sitaram Arkalgud (SEMATECH); row left and center, respectively: Chairman Dr. Peter Ramm and co-chair Rolf Aschenbrenner (Fraunhofer IZM)

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Enabling Technologies for Green Electronic Packaging

Submitted by Dr. Mali Mahalingam, Tutorial Committee Chair,
IEEE CPMT Society Phoenix Chapter
mali.mahalingam@freescale.com

In our modern day living we are all very much aware of the waste materials we create, improper disposal of products at the end-of-life and many health and environmental consequences resulting from such actions. According to the UN Environment Programme, electronic waste totals 50 million tons a year worldwide ["High Tech Trash", National Geographic, Jan. 2008]. In the electronics industry this is a growing problem due to "rapid technology changes" and the practice of "planned obsolescence" in consumer electronic products. If the waste material is not properly recycled and treated, they become major sources of toxins and carcinogens. To combat the situation, RoHS (Restriction of Hazardous Substances) Directive came into effect in 2003 and this directive restricts the use of six hazardous materials in the manufacture of electronic and electrical equipment. We need to be more thoughtful and creative in the future in reducing and/or eliminating the use of harmful materials as we develop new materials, new assembly/manufacturing processes and new products.

IEEE CPMT Society Phoenix Chapter is organizing a half-a-day technical tutorial under the leadership of Dr. Mali Mahalingam of Freescale Semiconductor Inc., Tempe, Arizona, to focus on the theme of "Enabling Technologies for Green Electronic Packaging". It is planned for mid Sept. 2008, at Amphitheater, Airport Hilton, Phoenix. Following four topics are planned: (i) Pb free solders (ii) Green polymers for electronic packaging (iii) Environmentally friendly assembly/manufacturing processes and (iv) recycling/ environmentally friendly disposal. Dr. Darrel Frear (Freescale Semiconductor Inc.), Prof. C.P. Wong (Georgia Tech.), Dr. Luu T. Nguyen (National Semiconductor Inc.) have commit-

ted to be presenters. Commitment from a fourth speaker is shortly expected.

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Summary Report on ITHERM 2008

<center>Yogendra Joshi, Program Chair</center>

The ITherm 2008 conference was held at the Hilton at Walt Disney World Resort in Orlando, Florida during May 28-31, 2008. The Conference General Chair was Dr. Tom Lee from TSMC, Inc. and Program Chair was Prof. Yogendra Joshi from Georgia Institute of Technology. The conference was attended by approximately 260 registered attendees and included nearly 170 technical paper presentations.

The conference began on May 28 with a total of thirteen advanced short courses (4 hours each) and tutorials (2 hours each) presented by expert instructors in morning and afternoon sessions. In general, the short courses covered established topics of general interest, whereas the tutorials covered emerging themes. During May 29-May 31, the technical papers were presented in 38 sessions covering four Tracks: Thermal Management, Mechanics and Materials, Emerging Technologies, and Energy Efficient Electronics. The last of these, is a newly established topic of significant current interest. All papers in this Track were presented in the form of posters in a single dedicated session on May 30. In all, 18 technical sessions were held in Thermal Management, 8 in Mechanics and Materials, 6 in Emerging Technologies, and 6 in Energy Efficient Electronics.

In addition to the technical papers, there were three Keynote/Invited presentations. The opening Keynote titled, "Emerging Systems Packaging Technologies", was delivered on the morning of May 29 by Prof. R.R. Tummala from Georgia Institute of Technology. The ITherm Achievement Award Luncheon talk titled," IBM, Mainframes, and Environmentals", was delivered by Dr. R.R. Schmidt from IBM. There were four panel sessions during the conference. These included: "Thermal Management Challenges for Military Electronics", "Cooling Challenges and Energy Efficiency in Low Form Factor Electronics", "Cyber Infrastructure Resources for Thermal Management", and ""Energy Efficient Data Centers".

A key feature of the ITherm conference has historically been the link with the Electronics Components and Technology Conference (ECTC) through the joint Exhibits program. This year the distance between the two venues required the use of shuttle buses. Visits to the Exhibit were arranged for the evening reception on May 28, and during the afternoon of May 29. For ITherm 2010, the proximity of the two conference venues will make this linkage even stronger.

The Awards Luncheon was the final event of the conference, held on May 31. At this event, Best Paper Awards to the authors of the highest rated paper from each of the four Tracks were presented. In addition, two papers from the Thermal Track and one from the Mechanics Track received the Outstanding Paper Awards.

SCV CPMT Chapter – Aaargh!

The theme of CPMT's luncheon at ECTC this year was "Pirates!" with the idea that there is treasure buried within the Society's services and networking. After returning to the Santa Clara Valley (CA), several of the ECTC attendees (along with others from the chapter's operating committee) celebrated by donning some of the booty brought back from the Conference.

SCV Chapter OpCom members (from left): Valerie Pilloud (treasurer), Allen Earman, (vice-chair), Paul Wesling (chapter advisor), Mudasir Ahmad (secretary), Janis Karklins (membership development), Bernie Siegal (SEMI-THERM liaison); front row: Ed Aoki (program co-chair), Sandra Winkler (program co-chair)

The SCV Chapter is holding their summer planning meeting/picnic at the home of Bernie Siegal in July to structure another active program for 2008-2009.