

## ESTC 2008

2<sup>nd</sup> Electronics System-Integration Technology Conference  
1<sup>st</sup> – 4<sup>th</sup> September 2008, Greenwich, London, UK

[www.estc.biz](http://www.estc.biz)

The IEEE 2<sup>nd</sup> ESTC Electronics Systems-Integration Technology Conference is on track to be an outstanding technical event and exhibition. ESTC-2008 will comprise 270 themed technical papers in six parallel oral tracks and posters. Posters will be displayed and also be presented.

The Technical themes at ESTC-2008 are:

- Advanced Packaging
- Emerging Technologies
- Manufacturing and Test Technology
- Modeling, Simulation and Design
- New Materials and Processes
- Power Electronics
- Technology & Reliability for Micro and Nano Systems
- Assembly of Alternative Energy Sources
- Optoelectronics
- Electronics system-integration for healthcare.

### Special invited Sessions:

**Asia-Pacific Photo-voltaics** will address: • “Third Generation Photo-voltaics” • “System-integration Strategies for co-Generation of Electricity, Heating and Cooling using Solar Photo-voltaic Modules” • “Building Integrated Photo-voltaics for Maximum Power Generation” • “The Intellectual Property Landscape for Photovoltaic Technologies”

**Standards** will address: “The Critical Standards for BT’s 21<sup>st</sup> Century Network” • “EMC and Functional Safety Requirements for Integrated Electronics Systems” • “The Evolution of Standards in Industry”

**Prognostics and System Health Management for Reliability** will address: “Embedded Prognostics and Health Monitoring Systems” • “Integrated Vehicle Health Management in the Auto Industry” • “Aerospace and Electronics System Prognostic Health Management” • “Detecting Anomalies in Field Returned Laptops using Mahalanobis Distance”

**Greening the Blue Planet (public session):** • “Electronics, Energy and the Environment” Johns Hopkins University • “Interdependence of Marine Ecosystems and Climate Change” WWF • “Future Parks in Future Climates - scalable solutions” Ecologist Brecon National Park • “Talking Green about Nuclear” University of Cardiff

### Short Courses

Eight half-day short courses will be taught on Monday 1<sup>st</sup> September

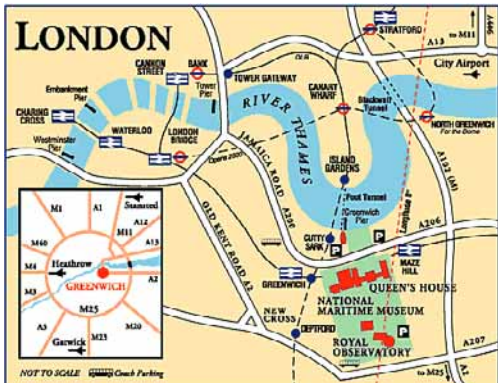
### Opening and Keynotes

The Conference will be opened on Tuesday 1<sup>st</sup> September by Baroness Blackstone, Chancellor of the University of Greenwich. The Keynote Opening Address will be on “**Ambient Assisted Living**” by Dr. Nakita Vodjdani, Vice-President of the European Union AAL Association. The Keynote closing address will be by Prof. Peter Cochrane, entrepreneur and former Chief Technologist of British Telecom

**Attendance is expected to exceed 500 international delegates.**

**The major technical exhibition will be held alongside the Conference – an excellent opportunity for suppliers of materials, design houses, circuit manufacturers to promote their products and reach potential customers.**

**ESTC 2008** will be held at Greenwich, a World heritage site and major maritime site on the banks of the River Thames in the magnificent city that is London. The Conference and Exhibition will be hosted by the University of Greenwich in the buildings of the former Royal Naval College. Plenary sessions will be in the Great Painted Hall – providing a wonderful ambience for the technical presentations.



Visit: [www.estc.biz](http://www.estc.biz)

Information: [sinnadurai@estc.biz](mailto:sinnadurai@estc.biz)

Joint International Congress and Exhibition  
In Conjunction with the 1st World ReUse Forum



### Merging Technology and Sustainable Development

September 07-10, 2008 Berlin, Germany

Organized by Fraunhofer IZM

Technical Co-sponsor: CPMT Society

Industrial sponsors: DELL, Intel, Panasonic

Building on the tradition of the extremely successful conferences **Electronics Goes Green 2000** and **2004, Electronics Goes Green 2008+** will again be the meeting point for specialists from all over the world working in the realm of electronics and the environment. This year's presentations will focus on the following main topics:

- Legislation: Impacts, Improvements & Harmonization
- Products, Systems & Sustainable Technologies
- Management & Social Responsibility

If you have a professional interest in the best environmental solutions already or if you are increasingly forced into dealing with topics like energy efficiency, carbon footprints, toxic substances or recycling, then the Electronics Goes Green 2008+ is the place to come for updates and international exchange.

Visit our website for the Preliminary Program or subscribe for conference newsletter:

[egg2008.izm.fraunhofer.de](http://egg2008.izm.fraunhofer.de)

*Call for Papers posted .... EDAPS 2008*

## Electrical Design of Advanced Packaging and Systems Symposium

- Seoul, Korea - December 10-12, 2008

- Abstracts Due July 31

Technologists are requested to submit papers in the areas of Modeling, Design, and Measurement of:

- High-speed Digital Signal Integrity
- Power Distribution Network
- High-speed Channels and Interconnect
- Embedded Passives - EMI/EMC
- System in Package (SiP) / System on Package (SoP)
- RF/Microwave Packaging

For more information, please visit our website:

[edaps2008.org](http://edaps2008.org)

Contact: Prof. Dr. Joungho Kim, KAIST, Symposium Chair,  
[joungho@ee.kaist.ac.kr](mailto:joungho@ee.kaist.ac.kr)

# Polytronic '08

Co-located with  
**PORTABLE'08**



## 7th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics

Garmish-Partenkirchen, Germany 17-22 August, 2008

Please join researchers, engineers and scientists from around the world in mid-August 2008 to share knowledge and experience in Polymeric Materials for Microelectronic & Photonic Applications (POLY), Adhesives in Electronics, and Polymeric Electronics Packaging (PEP). The program will include keynote, invited and contributed presentations, as well as panel discussions. There are eight half-day tutorials and an IEEE Pavilion featuring technology exhibits and demonstrations.

For the Program and registration details for both Polytronic and PORTABLE, please visit:

[www.polytronic2008.com](http://www.polytronic2008.com)

## Workshop on Accelerated Stress Testing & Reliability

October 29-31, 2008 Portland Oregon

Theme: "Achieving Cradle to Grave Reliability  
using DFR and AST"

The ASTR Workshop is an annual CPMT gathering of test and reliability engineers focused on accelerated stress testing and its relationship to reliability. It provides a forum for people from many different disciplines to network and discuss related issues and methodologies. Over the last few years, Accelerated Stress Testing & Reliability (ASTR) has been embraced by an ever widening array of worldwide companies seeking to reconcile the need for the highest quality product with the necessary push for early time-to-market.

Registration is now open – save through Sept. 30th.

Please visit:

[www.ewh.ieee.org/soc/cpmt/tc7/ast2008](http://www.ewh.ieee.org/soc/cpmt/tc7/ast2008)



IEEE  
COMPONENTS, PACKAGING,  
AND MANUFACTURING  
TECHNOLOGY SOCIETY



**Final Program**  
**Future Directions in IC and Package Design Workshop (FDIP)**

**October 26, 2008, San Jose, CA**

sponsored by:

organized by:

**CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)**

**SESSION I: SYSTEM DESIGN**

Session Chair: Paul D. Franzon, – North Carolina State University

Architecture Implications of 3D Integration Technology – Michael Ignatowski, IBM Corporation  
Design Considerations for Highly Integrated 3D SiP for Mobile Applications – Joungho Kim, KAIST Korea  
Design of Through-Silicon Vias and Vertical Shielding for 3D Integration - Ivan Ndip, Fraunhofer IZM, Germany  
Tb/s-Class Module-to-Module Optical Data Buses on Printed-Circuit Boards - Fuad Doany, IBM Corporation

**SESSION II: MODELING**

Session Chair: Albert E. Ruehli, IBM Corporation

Electromagnetic Solvers for Interconnect and Package Modeling – New Developments – Sadasiva M. Rao, Auburn University  
Accelerated Parallelized Integral Equation Techniques for Packaged Microelectronics – Vikram Jandhyala, Univ of Washington  
Benefits of Surface Integral Equation Modeling Leveraging Massively Parallel Advanced Techniques – Jason D. Morsey, IBM

Workshop will be held at the Wyndham Hotel, 1350 N. 1st Street, San Jose, California 95112, (408) 453-6200. The hotel is holding a block of rooms for participants at a special rate of \$119.00 plus tax. Room reservations must be made by **September 25, 2008** to guarantee this rate. After that time rooms will be on a space and rate available basis only. *Be sure to mention that you are attending the Electrical Performance of Electronic Packaging conference.* Rooms are limited so make your reservations early. Additional information can be obtained at [www.epep.org](http://www.epep.org)

Additional information may be obtained from the workshop chairs:

**Alina Deutsch**

deutsch@ieee.org  
phone: (914) 945-2858  
fax: (914) 945-2141

**Madhavan Swaminathan**

madhavan.swaminathan@ece.gatech.edu  
phone: (404) 894-3340  
fax: (404) 894-9959

and the workshop administration:

epd@enr.arizona.edu  
phone: (520) 621-3054  
fax: (520) 621-1443

Attendees interested in the workshop will be charged a \$60.0 fee that will cover afternoon refreshments, digest of abstracts, and posting of the foils on the CPMT Society TC-EDMS web site. All attendees must register by September 12, 2008 using the EPEP'08 website at [www.epep.org](http://www.epep.org) in order to assure that the workshop is being held. On-site registrants will be admitted depending on availability of seating.



## 59th ECTC Call for Papers

### First Call For Papers 59th Electronic Components and Technology Conference [www.ectc.net](http://www.ectc.net)

**To be held in San Diego, California, USA, May 26 - May 29, 2009**

The Electronic Components and Technology Conference is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. The ECTC is jointly sponsored by the Components, Packaging and Manufacturing Technology Society of the IEEE and the Electronic Components Association. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the following areas:

#### Advanced Packaging:

New packaging technologies, systems packaging, first level thermal solutions for high power applications, designs, materials, and configurations addressing performance, density and cooling for single chip, multichip and SIP, waferlevel, MEMS and power packages. Special emphasis on flip-chip, fine pitch and high lead count packaging in CSP, BGA, CGA, LGA and SMT packages for both Pb-based and Pb-free bumps and package assembly.

#### Electronic Components & RF:

Discrete Passive Components; integrated and embedded passive and active components integration on silicon ceramic, organic substrates; electronic components-design, materials, processing, test, characterization; new technology development for components - silicon through vias, wafer level RDL, nano materials and processes; tunable materials, structures, devices and switches; RFID/sensors, RF MEMS, integrated antennas, filters, baluns; components and modules for WLAN, UWB, mobile PC and multi band radio applications.

#### Emerging Technologies – Biomedical, Nano-Scale and Organic Devices Packaging & Portable Power Supply:

All design, fabrication, modeling, and performance aspects of materials, devices, systems, and packaging in the areas of: (1) Nanoelectronics including <90nm Si device technology, Single Electron Transistors (SETs), Carbon Nano Tube (CNT)/nanowire and molecular devices, spintronics, etc., (2) Bioelectronics such as biomedical, bioengineering, biosensors and electronics for medical devices, and (3) Organic /Printable Electronics.

#### Interconnections:

Interconnect innovation/design/process on all packaging levels including wire bonding, flip chip, 3D and through Si via connections, first-level package, and printed circuit board. Topics may range from bump and under bump metallurgy, electromigration, conductive polymers and nano material based interconnects, novel enabling techniques, electrical performance, to environmental concerns.

#### Manufacturing Technology:

Advanced process and equipment improvement for volume production of emerging technologies including: system in package, package on package, wafer thinning, bumping, stacking; low-k chip, Pb-free and MEMS packaging. Product level rapid integration and system level optimization of new packaging technologies focusing on cost, yield, electrical/mechanical/ environmental performance, supply chain development, and product ramp.

#### Materials & Processing:

Materials and processes for IC and microsystems packaging that enhance mechanical, thermal and electrical performance and cost effectiveness. This includes advances in materials and processing of adhesives, encapsulants, nanomaterials, chip underfills, solders and alloys, magnetic and optical materials, thermal interface materials, polymers, ceramics, composites, flexible dielectrics and substrates, thin films, coating, bonding, plating and assembly processes.

#### Modeling & Simulation:

Electrical, thermal, optical, and mechanical modeling, simulation, and characterization of packaging solutions including system-level applications. Example topics include - assembly manufacture modeling, Cu low-K interconnects, drop impact models, embedded passives, equivalent circuit models, fullwave modeling, lead-free solders, macromodeling, measurements, and thermomechanical reliability.

#### Optoelectronics:

Packaging and technology for fiber-optic modules, components and devices including: amplifiers, transmitters, receivers, integrated photonics, passive components, plastics packaging, chip to chip, backplanes and storage. With special emphasis on transceivers, optical inter-connects, high power lasers, advanced processes, manufacturing technology, micro-optical packaging, LED/laser projection displays and solid state lighting.

#### Posters:

Papers may be submitted on any of the major topics listed by the subcommittees. Presentation of papers in a poster format is highly encouraged at ECTC.

#### Quality & Reliability:

Reliability assessment and prediction at the system, PWB or package level; reliability testing and data analysis; failure analysis of field and test failures; reliability modeling of accelerated testing; reliability issues in emerging technologies; interconnect reliability physics, testing and predictive simulation; advances in reliability test methods and failure analysis.

**At the discretion of the program committee, submitted abstracts may be considered for poster presentation.**

You are invited to submit a 750-word abstract that describes the scope, content, and key points of your proposed paper via the website at [www.ectc.net](http://www.ectc.net). If you have any questions, contact:

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Intel Corporation  
MS – CH5-263  
5000 W. Chandler Blvd., Chandler, AZ 85226  
Phone: +1-480-554-5202  
Fax: +1-480-554-7171  
Email: [rajen.c.dias@intel.com](mailto:rajen.c.dias@intel.com)

#### Abstracts must be received by October 15, 2008.

All abstracts must be submitted electronically at [www.ectc.net](http://www.ectc.net). You must include the mailing address, business telephone number, FAX number and email address of presenting author(s) and affiliations of all authors with your submission.

#### Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200 word proposals must be submitted via the website at [www.ectc.net](http://www.ectc.net) by **October 15, 2008**. If you have any questions, contact:

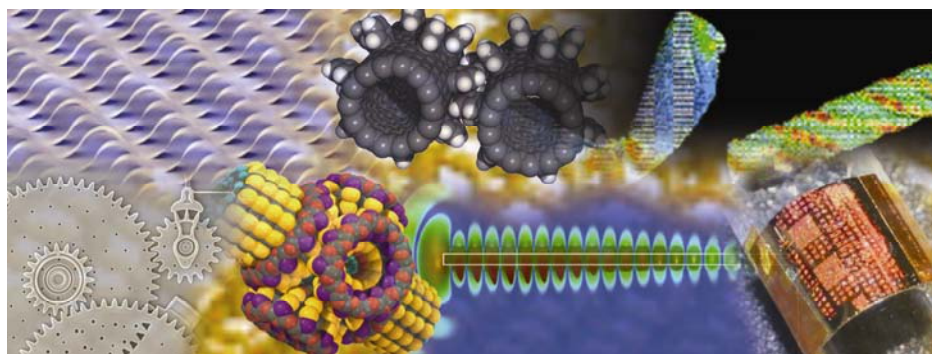
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# Institute of Electrical and Electronics Engineers, Inc.

**Phoenix Section**  
**Components, Packaging and**  
**Manufacturing Technology**  
**Society Chapter**  
**&**  
**Waves and Devices Chapter**

*PRESENT AN ALL-DAY  
 WORKSHOP ON*



Images courtesy of Argonne National Laboratory, NASA Ames Center for Nanotechnology, Stanford University, Sandia National Laboratories (SUMMIT™ Technologies) and Nanorex, Inc.

## Emerging Device and Packaging Technologies

*Friday, November 14<sup>th</sup>, 2008 7:00 A.M. – 5:00 P.M.*

*Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)*

### EXECUTIVE COMMITTEE

#### Workshop Chair

Vasu Atluri, Intel  
[vpatluri@ieee.org](mailto:vpatluri@ieee.org)

#### Workshop Co-Chair

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#### Registration Chair

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#### Vendor Committee Chair

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#### Electronic Media Chair

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#### Arrangements Chair

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Co-Chair: Mel Miller, Freescale  
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Henning Braunisch, Intel  
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 Sanka Ganesan, Intel  
 Steve Goodnick, ASU  
 Vivek Gupta, Freescale  
 Sunit Mahajan, Intel  
 Steve Rockwell, Motorola  
 Kalluri Sarma, Honeywell  
 Sudhama Shastri, CMD  
 Sandeep Tonapi, Anveshak

### Call for Papers

The continued scaling of microelectronics for mainstream applications such as computing and communications on one hand has been enabled by newly developed materials, tools, and techniques; on the other hand the associated capabilities are spawning novel applications and market opportunities. This year's one-day workshop focuses on the topics of nanotechnology, bioelectronics, and energy. Invited experts from industry, academia, research labs, and consortia will share their vision of technical challenges and opportunities in these areas. Current and emerging device, interconnect, and packaging technologies will be discussed in depth. A poster session on the broader workshop topic of emerging device and packaging technologies has been added this year to provide additional presentation and discussion opportunities. Select vendors will exhibit products and services related to all aspects of the supply chain for microelectronics design and manufacturing.

### Invited Speaker Topics

#### Nanotechnology

- Nanofabrication
- Nanoelectromechanical Systems
- Nanofluidic Devices

#### Bioelectronics

- Biochips
- Biosensing
- Biosecurity

#### Energy

- Solar Cells
- Energy Harvesting
- Micro Power Generators

### Poster Session

Abstracts are invited for consideration to the poster session in emerging device and packaging technologies (not limited to nanotechnology, bioelectronics, or energy).

**Poster Abstract Submissions:** Two pages (topic, summary of significant results and conclusions – WORD or PDF files only). Abstract must include author names, affiliations, addresses, and e-mail address of lead author.

|                          |  |
|--------------------------|--|
| Submission Deadline:     | August 29, 2008  |
| Submitting Address:      | <a href="mailto:melmiller@ieee.org">melmiller@ieee.org</a> |
| Acceptance Notification: | September 19, 2008   |
| Final Presentation Due:  | November 5, 2008   |

**Sponsorships and Vendor Displays:** This is a great opportunity to promote your company or product. For more information, contact Vasu Atluri [vpatluri@ieee.org](mailto:vpatluri@ieee.org) or Chuck Weitzel [c.weitzel@ieee.org](mailto:c.weitzel@ieee.org) (sponsors) and Steve Rockwell [steve.rockwell@ieee.org](mailto:steve.rockwell@ieee.org) (vendors).

**Workshop Registration:** On-line registration will open in August at [www.acteva.com/go/ieeephxsecworkshop2008](http://www.acteva.com/go/ieeephxsecworkshop2008)

## **33<sup>RD</sup> INTERNATIONAL ELECTRONICS MANUFACTURING TECHNOLOGY CONFERENCE IEMT 2008**

**4th-6th November, 2008**

**Parkroyal Hotel, Penang, MALAYSIA**

The 33rd International Electronics Manufacturing Technology (IEMT) Conference is the premier IEEE event devoted to the manufacture of electronic, opto-electronic and MEMS/sensors devices and systems. IEMT is an established International conference of long standing organized by the Components Packaging and Manufacturing Technology (CPMT) Society of IEEE. IEMT 2008 is being organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from CPMT's Santa Clara Valley Chapter.

IEMT 2008 will feature short courses, technical sessions, and exhibitions. It aims to provide good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation. IEMT 2008 is an international forum, providing opportunities to network and meet leading experts. Since the 1980's and 1990's, IEMT has gained a reputation as a premier electronics materials and packaging conference and is well attended by experts in the field of electronic packaging from all over the world.

**Visit our website:** [cpmt.ieeemalaysia.org](http://cpmt.ieeemalaysia.org)



## **Semiconductor Thermal Measurement and Management Symposium**

**Fairmont Hotel, San Jose CA USA March 15th-19th, 2009**

### **CALL FOR PAPERS**

SEMI-THERM is the world's premier forum specifically dedicated to thermal management of electronics. The symposium fosters the exchange of knowledge between industry academics, experts and practitioners on the latest advances in electronics thermal management.

SEMI-THERM is soliciting papers on current thermal management technologies and practical application issues, modeling and measurement of electronic components and systems in the following areas:

#### **Component to System level thermal management:**

Die, Package, Board and Systems Level

#### **Packaging Materials:**

Interface, Spreading, Nanotechnology, Material Characterization, Composites

#### **Modeling and Analysis:**

CFD, Compact, Finite element, Thermal Limitations

#### **Cooling technologies:**

Conduction, Convection, Radiation, Air, Liquid, Two Phase, Fans and Blowers, and Solid State

#### **Applications:**

Consumer, High Volume, Harsh Environments, LED, Medical, Telecom, Portable, Automotive, Solar Photovoltaic, Military, Power and Storage Systems

Selection of papers for presentation is solely based on the extended abstract. The abstract should provide a complete summary of the proposed paper comprising work or result not previously presented or published.

The abstract should be between 2 and 5 pages of single spaced text giving the key results, findings and conclusions, supported by additional pages of figures, tables and references as appropriate. Abstracts must demonstrate that proposed papers are appropriate for SEMI-THERM and of high technical quality.

#### **Author Deadlines**

Abstract Deadline:

**September 15, 2008**

Abstract Acceptance Notification: **November 1st, 2008**

Photo-ready Full Manuscript Due: **December 15th, 2008**

Plan to attend and consider giving a paper –

Visit our website:

[www.semi-therm.org](http://www.semi-therm.org)

## **IMPACT 2008:**

**3rd International Microsystems, Packaging, Assembly and Circuits Technology**

held jointly with **EMAP 2008:**

**10th International Conference on Electronics Materials and Packaging**

**October 22 to 24, 2008**

**Taipei Nangang Exhibition Hall**

***"Creative Collaboration, More Than Packaging"***

Organized by IEEE CPMT-Taipei, ITRI, IMAPS-Taiwan, ISU University, SMTA and TPCA, the 3rd IMPACT and the 10th EMAP Joint Conference and TPCA Show 2008 are expected to bring together scientists, engineers and experts actively engaged in research and development on Microsystems, IC Packaging, Assembly, Materials and PCBs to discuss the current progress and emerging technologies in the fields

**Plan now to attend. Visit:**

**[www.impact-emap.org](http://www.impact-emap.org)**

## **2nd Int'l Conference on Thermal issues in Emerging Technologies, Theory and Applications (ThETA2)**

**December 17 – 20, 2008 Cairo, Egypt**

**Papers due: July 31, 2008**

Emerging Technologies in various domains, including Microelectronics, Nanotechnology, Smart Materials, Micro-Electro-Mechanical Systems, Biomedical engineering as well as New Energies, all raise many issues related to thermal effects and interactions. The importance of such effects is continuously increasing to a point where they become a dominant factor in determining the performance of such technologies.

Parallel to the conference, a set of workshops will be conducted, aiming at disseminating advances made in different areas to the academic and industrial public in Egypt, fostering network creation with renowned international research centers as well as giving an impulse to academic/industrial cooperation.

Find out more! **Contact:** [thetacnf@gmail.com](mailto:thetacnf@gmail.com)

## **IEEE Components, Packaging and Manufacturing Technology Society**

Marsha Tickman, Executive Director  
PO Box 1331 / 445 Hoes Lane  
Piscataway, NJ 08855 USA

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