60 kHz, and applied those measurement methods to understanding and solving other problems in ultrasonic bonding machines and processes. Later, he used a laser interferometer to refine those earlier measurements. In 1971 he started the ASTM F-01.07 committee to standardize wire bond testing methods, which included pull test, nondestructive test, and ball bond shear test. Also, standards for bonding wire inspection methods, etc., were developed during that period. Harman, who currently chairs ASTM Committee F-01.07 (Wire Bonding, Flip Chip, and Tape Automated Bonding), updated and re-balloted the original wire bonding standards in 2005-06. Note that Harman's IEEE fellow citation (in 1982) was "for development of process control and screening procedures for microelectronic welding and bonding". He continues to contribute to the wire bonding area. Recently, an extension of his laboratory work and publications on wire bonding to soft substrates led to applying those principles to wire bonding on Cu-LoK chips. Other recent publications discussed projected metallurgical wire bond problems in NASA extreme temperature planetary exploration probes.

During the 1970's, Harman contributed to the military standards for testing wire bonds (at that time these were the only semiconductor/packaging standards publicly available and in general use), attended JEDEC meetings, and contributed data to be incorporated in their standards. He wrote the bond pull test method for MIL-S-19500 which was subsequently added to MIL-STD-750C, and supplied data and curves for the most used wire bond pull test in MIL-STD-883. He wrote the first version of the nondestructive bond pull test in MIL-STD-883 and has defended its use numerous times, and his paper on that subject in the IEEE IRPS stands alone for the statistical and metallurgical understanding of that test method. Currently, that test is required for most critical parts flown by NASA.

In his NIST Fellow position, George Harman has served as a national and international consultant in the field of wire bonding, advising and solving problems in chip-package interconnections for numerous organizations each year. He has taught most US and many foreign engineers both metallurgical and practical aspects of wire bonding in the 8-hour short-courses sponsored by UAZ, IMAPS, HKUST, and many others organizations for 20 years. He used the well developed and organized content of such lectures, in 1989, and published the first edition, and in 1997 the second edition of the only book(s) on that subject. It is frequently referred to as "the wire bond bible" and has been used by thousands of engineers (over 5000 copies of second edition have been sold by McGraw Hill). Two wire bond manufacturers have given a copy with each major machine purchased ("to educate and save us time and service calls to our customers"). These books have been a major world-wide contribution to the field by Harman.

Most of George Harman's career has been engaged in understanding, standardizing, implementing improvements into the industry's tooling, and disseminating wire-bond technology. He is the individual most responsible for transforming a labor-intensive manual bonding technology whose results depended upon an operator's skill, with attendant poor reliability, to a well-understood, highly automated (>8 bonds per second) method with an outstanding reliability record. As a result of Mr. Harman's work, wire bonding has become the industry standard. It accounts for more than 95 percent of the interconnections made between chips and the next level of assembly in electronic products manufactured worldwide. Approximately 7x10(+12) wire bonds are created each year. George Harman's work has had a profound impact on the industry, and likely benefited anyone utilizing an electronic product.
George's award will be presented at the 2009 ECTC.

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Book Reviews:

Introduction to System-On-Packaging (SOP), Miniaturization of the Entire System

By Rao R. Tummala and Madhavan Swaminathan
MacGraw-Hill, 2008, pp. 785

This is a complete introduction to the on-going research and development of SOP. The authors have co-authored several chapters and edited the rest written by leaders in the field. The basic theme is that there is plenty of room for further miniaturization even after the IC digital evolution call Moore's Law. There is no question that the many components and boards of a system are undergoing continual miniaturization using techniques other than those from the CMOS juggernaut. However, the transistor count has gone up 9 orders of magnitude and the transistor miniaturization improved by 6 orders, whereas the SOP miniaturization appears limited to 2 orders (may just be the reviewers conservative view). None the less, all this technology will be needed to win in the marketplace over the next decade.

This book describes where SOP technology is being expanded and directions technology may take, but does not really address any economic destiny. Remember CMOS is slowing for economic not technical reasons. The SOP is not an irresistible BORG spaceship assimilating all technology in its integration effort, but one future direction proved plausible by the many great developments discussed in this book. Many university and industrial advances are presented in detail within this book.

Before discussing the details, it is important to note that each section of this book presented new exciting facts and new technology interconnections to any reader except those with many years developing integrated packaging. The large number of "AHAs" is a mark of a great tech book.

The integration of unusual single MEMs or photonic element into a highly integrated system is quite a challenge. The MEMs and Optoelectonics chapters in this book give several options to accomplishing this level of integration in addition to discussing economic packaging of single MEMS and photonic devices. Other chapters address many integration aspects of Biosensor, electrical module testing, thermal management, wirering, RF, mixed signal, and stacked ICs.

The RF chapter uses LTCC and LCP integrated packaging as the basis for SOP creation. Particularly informative discussions occur on how to miniaturize and add gain to module antennas. Discus-

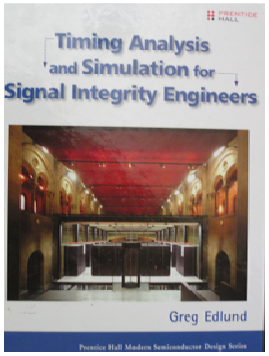
sion of RF MEMs switches and their pros and cons as well as popular RFIDs are also well covered.

One practical aspect of system realization is not discussed in the book (it may be too soon). With the existing system of miniaturizing / integrating the digital and small signal analog signals in integrated circuits and interconnecting them with other components on boards there are well established methods to modify (tweak) the design on the board level when the simulations missed a little in timing or noise levels. The higher level of miniaturization of SOP does not appear to have these options so may require higher fidelity simulations.

In addition to clear descriptions and explanations, each chapter has extensive references so that the working developing engineer can quickly study the foundation of any aspect of this field before they invest in further efforts. This book is a pleasant necessity for any engineer or manager involved in miniaturization of systems and modules.

Timing Analysis and Simulation for Signal Integrity Engineers

By Greg Edlund
Prentice Hall Modern Semiconductor Design Series
2008, 250 pages



This book would make a fine supplementary text to a prototype design course, however more use will be made of this book by a working engineer associated with a design that has small design margins and needs a mid project re-design. The author makes many humorous comparisons between what the company needs right now versus the time good design methods require. This tone revives the beaten down engineer into returning to the good path. He understands the pressures but guides the reader to know "when the design is ready to build." The book is more like a mentor and less prescriptive.

The book stresses in detail the I/O circuits which are pivotal to the signal integrity issue as well as the need to do 3D EM simulation of the package, components, and interconnections. "In the years ahead, the most successful signal integrity engineer will be those who are able to expand their vision beyond voltage and currents and into the realm of electromagnetic fields." For example, he details the study of a Land Grid Array interface and a SMA connector. The 3D modeling approach described is intended also for multichip modules, printed wiring board, sockets, connector cables, flex circuits, terminators, filers, and passive components. Most of the book is written as if the circuit designer does not have substantial input to the chosen packaging and interconnect technology so that one must compensate for the worst choices of others. However, after a designer masters this book it is hard to believe they will not be listened to by the packaging members of the design team.

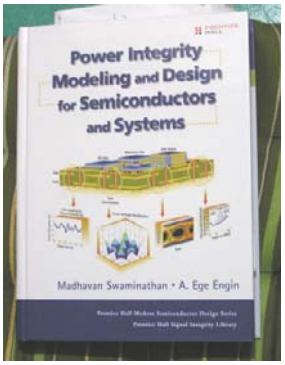
Although the text examples allow the reader to perform similar methods to their specific module, you are reminded regularly that one must establish their own "bag of tricks" based on their particular business. In addition, knowing when each trick is best called upon is the wisdom between the lines of this book. For example, admitting that one can not model every net in the circuit in great detail, he presents a list of measures by which you can pick the nets most critical to your circuit. In another example, he differentiates when you can assign model making to the supplying vendor and when you had better do it yourself.

One exceptional feature of this book for those no longer used to final exams is the review appendices where one can quickly get up to speed on CMOS, SPICE, and Maxwell's equations. He also bases this book on software tools that most universities and companies have available: High frequency SPICE, Agilent's ADS, and CST Microwave Studio.

One favorite quote from the book … "job of engineer is to play role of seer…without becoming a whiner". In summary, if this is your business than this is your book.

Power Integrity Modeling and Design for Semiconductors and Systems

By Madhavan Swaminathan and A. Ege Engin
Prentice Hall Modern Semiconductor Design Series
2007



Most Electrical Engineering departments center their curriculum around circuit design. This CPMT Newsletter reviews design textbooks from the perspective of how the component, packaging, and manufacturing issues are integrated into the text design discussion. Based on our metric this textbook by Swaminathan and Engin receives good grades. The package design is completely integrated into the circuit design for the Power delivery network (PDN). The integration of package design with system design has been a strength of the Georgia Institute of Technology, home of the authors.

The student should feel confident in modeling a complex IC system and performing design trade-offs with explicit packaging design options upon completion of a course centered on this book. However, the professor centering a course around this book will have to provide the practical specifics of components and materials in any class projects since the book does not go down to this level of detail. For example, the planes in the power distribution network are described mathematically but are not made specific by customizing to LTCC, or LCP, or BCB-Cu.

Strong points of this book include frequent pertinent examples/problems within the chapters; listing of many different power and ground strategies to maintain integrity while CMOS logic is switching on a massive scale; and detailed examples from Sun Microsystems, IBM, National Semiconductor, Cisco, DuPont, Panasonic, and Rambus. It may be useful to review one of these commercial examples in the last chapter every time an important modeling skill is mastered in the earlier chapters so the student recognizes the power gained by each method.

While scanning the book, questions came up regularly but each time the answer was found only a few pages away demonstrating the tight organization of the material. One slight detraction was the constant use of 3-letter abbreviations with seldom a repetition of the originating phrase. Fortunately their excellent index serves well as a glossary.

This book will function well as a structured textbook for a course on modeling digital board level systems as well as a reference for a practicing engineer asked to design and model something a bit beyond normal expertise. The extensive references at the end of each chapter allow further digging into any topic needing further understanding for a particular application.

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Conference Reviews:

Conference Report from ESTC 2008

Submitted by Nihal Sinnadurai & Chris Bailey
Report & photos: **www.cpmt.org/docs/0809estc.pdf**

The 2nd Electronics System-Integration Technology Conference (ESTC-2008) was held at the magnificent buildings of the historic Old Royal Naval College on the banks of the River Thames in Greenwich, London from September 1-4, 2008. This premier international conference is held every two years in Europe and brings together scientists, engineers and managers in the field of micro and nano electronics, photonics, MEMS, and bio components, their integration and packaging.

ESTC-2008 was organised jointly by the University of Greenwich and the UK&RI Chapter of IEEE-CPMT and sponsored by CPMT-IEEE, the University of Greenwich, and supported by IMAPS-Europe. The conference compliments the corresponding CPMT global conferences ECTC and EPTC held in the USA and Singapore respectively and the European EMPC organised by IMAPS-Europe. The collaboration agreement in Europe results in us sharing alternate years for ESTC organised by IEEE-CPMT in Europe and EMPC organised by IMAPS-Europe. In this way we serve the interests of the delegates to provide ongoing major conferences without diluting the resource to deliver them.

The Executive and Technical Programme committees of the 2nd ESTC extend their sincere thanks to all the authors, presenters, short course instructors, session chairs, exhibitors, sponsors and delegates, who helped make ESTC-2008 a resounding success.

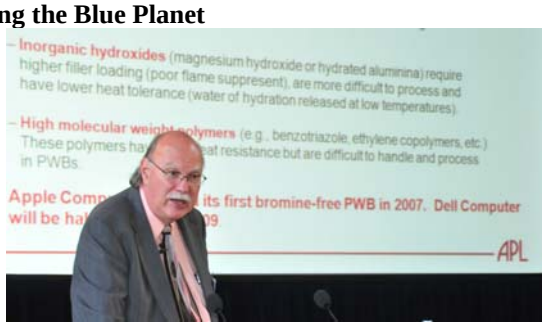
A Truly International Event

Contributions from 32 countries made ESTC-2008 a truly global conference. Authors from academia, industry and research institutes presented 252 papers at forty oral sessions and eight poster sessions to 384 delegates. Nine professional development courses attended by 67 participants on the preliminary day of the Conference added to the technical excellence of the event.

The strong technical range of the conference papers and courses covered the technical themes of Advanced Packaging, Emerging Technologies, Healthcare, Manufacturing & Test, New Materials and Processes, Modelling and Simulation, Optoelectronics, Reliability and special request topics such as Power Electronics and Assembly of Alternative Energy Sources. A themed technical exhibition with exhibits from 15 organisations, complimented the event and provided delegates with the opportunity to discuss commercial needs.

Special invited themes led and by international experts provided leading-edge insight in three technical themes on Prognostics and Health Management, Asia-Pacific Photo-Voltaics, and Standards, and a very special session on Greening the Blue Planet looked deeply into the impact and solutions that man and his technology has on the planet. 'When 'Technology Meets Market' provided constructive business decision insights from special panellists and knowledgeable delegates.

Greening the Blue Planet



Keynote lectures by Dr Nakita Vodjdani on the European Programme for Ambient Assisted Living, Dr Jean-Marc Yannou on SiP technologies and Dr Stuart Strickland who described Building Mobile Connectivity gave a great start to each conference day.
The anchor Closing Session was chaired by Nihal Sinnadurai, the Executive Chair of ESTC-2008 and Chair of IEEE-CPMT-UK&RI. The session was kicked off with the Challenging Keynote by Professor Peter Cochrane on 'The Challenge of the Non-Linear' during which he asserted that systematic, i.e. linear, approaches were inadequate for the complex technology challenges of the future.

The Challenge of the Non-Linear **Prof. Peter Cochrane**