14th International Memory Workshop

May 15th – 18th 2022

Hybrid Event (on-site and virtual)

Organizing Committee

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Rino Micheloni, University of Ferrara, Italy
Andrea Redaelli, STMicroelectronics, Italy
Tomoya Saito, Renesas, Japan
Tomoya Sanuki, Kioxia, Japan
Eitan Shauly, Tower Semiconductor, Israel
Shiva Shetti, Infineon, USA
Shuichiro Yasuda, SONY, Japan
Jane Yater, NXP Semiconductors, USA

Summary of Events

Hybrid On-Demand Event May 15th-18th : suggested schedule only (*time is CEST*)

Sunday, May 15th

Tutorial 1 – Ferroelectric Memories	09:00AM – 12:00PM
Tutorial 2 – 3D Memories – Security Aspects of Memories	02:00PM – 04:00PM

Monday, May 16th

Opening remarks	08:45AM – 09:00AM
Session #1 – Keynotes	09:00AM – 10:30AM
Session #2 – RRAM+PCRAM I	11:00AM – 12:15PM
Session #3 – Posters	02:00PM – 05:00PM
Reception	05:30PM

Tuesday, May 17th

Session #4 – MRAM+Ferro I	09:00AM – 11:05AM
Session #5 – Flash+3D-NAND	11:30AM – 12:45PM
Session #6 – RRAM+PCRAM II	02:15PM – 04:20PM
Panel Discussion	04:45PM – 06:45PM
Banquet	07:00PM

Wednesday, May 18th

Session #7 – MRAM+Ferro II	09:00AM – 10:40AM
Session #8 – Storage Memory+3D-NAND	11:10AM – 12:50PM
Closing Remarks	12:50PM

Sunday May 15th, 2022

Tutorials 09:00AM – 04:00PM

PART I – FERROELECTRIC MEMORIES

09:00AM – 12:00PM

Chairs: ***Dirk Wouters (RWTH Aachen)***
Katherine Chiang (TSMC)

Laurent Grenouillet,CEA-Leti, « Ferroelectric Random Access Memory (FeRAM) »

Halid Mulaosmanovic, GlobalFoundries, «Ferroelectric Field Effect Transistors (FeFET) »

Shosuke Fujii, Kioxia, « Ferroelectric Tunnel Junction (FTJ) »

PART II – 3D MEMORIES – SECURITY ASPECTS OF MEMORIES

02:00PM – 04:00PM

Chairs: ***Antonio Arreghini (imec)***
Thomas Mikolajick (Namlab/TU Dresden)

Onur Mutlu, ETH Zurich, « Security aspects of DRAM »

Swaroop Ghosh, Penn State University, « Security Aspects in Nonvolatile Memories »

Posters

[P1] Saurabh Suryavanshi, Cerfe Labs, “Extreme Temperature (> 200 C), Radiation Hard (> 1 Mrad/cm2), Dense (sub-50 nm CD), Fast (2 ns write pulses), Non-Volatile Memory Technology”

[P2] Lei Chen, Solidigm, “SSD Drive Failure Prediction on Alibaba Data Center Using Machine Learning”

[P3] Yuya Ichikawa, University of Tokyo, “Non-volatile Memory Application to Quantum Error Correction with Non-uniformly Quantized CiM”

[P4] Yannick Raffel, Fraunhofer IPMS CNT, “Endurance improvements and defect characterization in ferroelectric FETs through interface fluorination”

[P5] Ruben Alcala, NaMLab gGmbH, “Influence of Interfacial Oxide Layers in Hf0.5Zr0.5O2 based ferroelectric capacitors on reliability performance”

[P6] Sangsu Park, SK Hynix, “Recognition Accuracy Enhancement using Interface Control with Weight Variation-Lowering in Analog Computation-in-Memory”

[P7] Theophile Dubreuil, CEA-Leti, “A novel 3D 1T1R RRAM architecture for memory-centric Hyperdimensional Computing”

[P8] Weishen Chu, Western Digital, “An Analytical Model for Thin Film Pattern-dependent Asymmetric Wafer Warpage Prediction”

[P9] Tarek Ali, Fraunhofer IPMS CNT, “Study of Nanosecond Laser Annealing on Silicon Doped Hafnium Oxide Film Crystallization and Capacitor Reliability”

[P10] Akihiro Yamada, Tokyo University of Science, “Bi-directional read method to reduce SOT-specific read disturbance for highly reliable SOT-MRAM”

[P11] Po-Kai Hsu, Georgia Institute of Technology, “In-Memory 3D NAND Flash Hyperdimensional Computing Engine for Energy-Efficient SARS-CoV-2 Genome Sequencing”

Monday May 16th, 2022

Session #1 08:45AM – 10:30AM KEYNOTES

Chairs: *Dirk Wouters (RWTH Aachen)*
Thomas Mikolajick (Namlab/TU Dresden)

08:45AM **Dirk Wouters**, Opening Remarks
09:00AM **[1.1] Lars Heineck**, Micron, "NAND Flash status and trends"
09:30AM **[1.2] Johannes Müller**, GlobalFoundries, "From Emergence to Prevalence: 22FDX Embedded STT-MRAM for Consumer Grade and Beyond"
10:00AM **[1.3] Giuseppe Croce**, STMicroelectronics, "Non Volatile Memory in Advanced Smart Power technology: product requirements and integration solutions"
10:30AM Break

Session #2 11:00AM – 12:15PM RRAM+PCRAM I

Chairs: *Andrea Redaelli (STMicroelectronics)*
Kevin Garello (Spintec)

11:00AM ***Invited*** **[2.1] Gabriel Molas,** Weebit Nano, "High temperature stability embedded ReRAM for 2x nm and beyond"
11:25AM **[2.2] Sijung Yoo**, SK Hynix, "Structural and Device Considerations for Vertical Cross Point Memory with Single-stack memory toward CXL memory beyond 1x nm 3DXP"
11:50AM **[2.3] Matteo Baldo**, Politecnico di Milano, "Modeling Environment for Ge-rich GST Phase Change Memory Cells"
12:15PM Lunch

Session #3 02:00PM – 5:00PM POSTERS

Chairs: *Martin Lueker-Boden (Western Digital)*
Stephen Heinrich-Barna (Texas Instruments)

02:00PM **[3.1] P1**
02:10PM **[3.2] P2**
02:20PM **[3.3] P3**
02:30PM **[3.4] P4**
02:40PM **[3.5] P5**
02:50PM **[3.6] P6**
03:00PM Q&A Posters
03:20PM Break
03:50PM **[3.7] P7**
04:00PM **[3.8] P8**
04:10PM **[3.9] P9**
04:20PM **[3.10] P10**
04:30PM **[3.11] P11**
04:40PM Q&A Posters

Reception 05:30PM

Tuesday May 17th, 2022

Session #4 09:00AM – 11:05AM MRAM+FERRO I

Chairs: *Karl Hoffmann (Infineon)*
Martin Lueker-Boden (Western Digital)

09:00AM ***Invited*** **[4.1] Stuart Parkin**, MPI Halle, "Racetrack Memory: recent progress"
09:25AM **[4.2] Yandong Luo**, Georgia Institute of Technology, "Performance Benchmarking of Spin-Orbit Torque Magnetic RAM (SOT-MRAM) for Deep Neural Network (DNN) Accelerators"
09:50AM **[4.3] Milan Pesic**, Applied Materials, "Variability and disturb sources in ferroelectric 3D NANDs and comparison to charge-trap equivalents"
10:15AM **[4.4] David Lehninger**, Fraunhofer IPMS CNT, "Integration of BEoL compatible 1T-1C FeFET memory cells into an established technology"
10:40AM **[4.5] Nicolo Ronchi**, imec, "A comprehensive variability study of doped HfO2 FeFET for memory applications"
11:05AM Break

Session #5 11:30AM – 12:45PM Flash+3D-NAND

Chairs: *Stephen Heinrich-Barna (Texas Instruments)*
Haitao Liu (Micron)

11:30AM **[5.1] Yu-Hsuan Lin**, Macronix, "NOR Flash-based Multilevel In-Memory-Searching Architecture for Approximate Computing"
11:55AM **[5.2] Hitomi Tanaka**, KIOXIA, "Toward 7 Bits per Cell: Synergistic Improvement of 3D Flash Memory by Combination of Single-crystal Channel and Cryogenic Operation"
12:20PM **[5.3] Sana Rachidi**, imec and KU Leuven, "At the Extreme of 3D-NAND Scaling: 25 nm Z-Pitch with 10 nm Word Line Cells"
(Late News)
12:45PM Lunch

Session #6 02:15PM – 04:20PM RRAM+PCRAM II

Chairs: *Karl Hoffmann (Infineon)*
Martin Lueker-Boden (Western Digital)

02:15PM ***Invited*** **[6.1] Munehiro Tada**, NanoBridge, "NanoBridge Technology for Embedded Nonvolatile Memory Application"
02:40PM **[6.2] Joel Minguet Lopez**, CEA-Leti, "1S1R sub-threshold operation in Crossbar arrays for low power BNN inference computing"
03:05PM **[6.3] Christian Peters**, Infineon, "Reliability of 28nm embedded RRAM for consumer and industrial products"
03:30PM **[6.4] Gabriele Navarro**, CEA-Leti, "Multilayer Deposition in Phase-Change Memory for Best Endurance Performance and Reduced Bit Error Rate"
(Late News)
03:55PM **[6.5] Syed Alam**, Everspin, "Persistent xSPI STT-MRAM with up to 400MB/s Read and Write Throughput"
(Late News)
04:20PM Break

Panel Discussion 04:45PM – 06:45PM

Panel Host: **Tomoya Sanuki** (Kioxia)
Participants: **Manan Suri** (IIT-Delhi), **Ishai Naveh** (Weebit Nano), **Maarten Rosmeulen** (imec), **Johannes Müller** (GlobalFoundries), **Kishore Muchherla** (Micron)
"Are Emerging Memories Finally Emerging?"

BANQUET 07:00PM

Wednesday May 18th, 2022

Session #7 09:00AM – 10:40AM MRAM+FERRO II

Chairs: *Thomas Mikolajick (Namlab/TU Dresden)*
Kevin Garello (Spintec)

09:00AM ***Invited*** **[7.1] Daniel Worledge**, IBM, "Spin-Transfer-Torque MRAM: the Next Revolution in Memory"
09:25AM **[7.2] Nishtha Gaul**, GlobalFoundries, "A Physics based MTJ Compact Model for State-of-the-Art and Emerging STT-MRAM Failure Analysis and Yield Enhancement"
09:50AM **[7.3] Shinsei Yoshikiyo**, University of Tokyo, "Edge Retraining of FeFET LM-GA CiM for Write Variation & Reliability Error Compensation"
10:15AM **[7.4] Jaegil Lee**, SK Hynix, "Memory Window Expansion for Ferroelectric FET based Multilevel NVM: Hybrid Solution with Combination of Polarization and Injected Charges"
10:40AM Break

Session #8 11:10AM – 12:50PM Storage Memory+3D-NAND

Chairs: *Antonio Arreghini (imec)*
Haitao Liu (Micron)

11:10AM ***Invited*** **[8.1] Maarten Rosmeulen**, imec, "Liquid Memory and the Future of Data Storage"
11:35AM **[8.2] Sunghyun Yoon**, SK Hynix, "Highly Stackable 3D Ferroelectric NAND Devices : Beyond the Charge Trap Based Memory"
12:00PM **[8.3] Laurent Breuil**, imec and KU Leuven, "High-K incorporated in a SiON tunnel layer for 3D NAND programming voltage reduction"
12:25PM **[8.4] Alessio Spessot**, imec, "Thermally stable, packaged aware LV HKMG platforms benchmark to enable low power I/O for next 3D NAND generations"
12:50PM **Dirk Wouters**, Closing Remarks