15th International Memory Workshop

May 21st – 24th 2023

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Srivardhan Gowda, *Intel*, USA
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Summary of Events

Sunday, May 21st

Tutorial #1 – TCAD and Modeling	8:30AM – 12:00PM
Lunch (Provided)	12:00PM – 2:00PM
Tutorial #2 – DNA Memories	2:00PM – 4:00PM

Monday, May 22nd

Session #1 –Keynotes	8:30AM – 10:20AM
Session #2 – 3D NAND I	10:50AM – 12:05PM
Lunch (Provided)/Committee Luncheon	12:05PM – 2:05PM
Session #3 – 3D DRAM and selectors	2:05PM – 3:20PM
Poster Presentations	3:30PM – 4:00PM
Poster Session + Reception	5:30PM – 8:30PM

Tuesday, May 23rd

Session #4 – Ferro	8:30AM – 10:10AM
Session #5 – 3D NAND II	10:40AM – 12:20PM
Lunch (Provided)	12:20PM – 1:50PM
Session #6 – Systems, STT & RRAM	1:50PM – 3:30PM
Panel Discussion	4:00PM – 5:30PM
Banquet	7:00PM – 9:00PM

Wednesday, May 24th

Session #7 – Neuromorphic/In-mem	8:30AM – 10:10AM
Session #8 – 3D Processing	10:40AM – 11:30AM
Closing Remarks – Best papers awards	11:30AM – 11:50AM

Sunday, May 21st

Tutorial #1 8:30AM – 12:30PM TCAD and Modeling

Chair: **Antonio Arreghini**, *imec*

08:30AM **Stephan Menzel**, *Forschungszentrum Jülich*, "Modeling of ReRAMs based on the Valence Change Mechanism: From Atomistic to Circuit-Level Models"

09:30AM **David Esseni**, *University of Udine*, "Ferroelectric materials for novel nanoelectronic devices"

10:30AM *Break*

11:00AM **Franz Schanovsky**, *GTS*, "TCAD Modeling of 3D NAND Flash - Techniques and Challenges"

12:00PM *Lunch (Provided)*

Tutorial #2: 2:00PM – 4:00PM DNA Memories

Chair: **Jian Chen**, *Stanford*

2:00PM **Andres Fernandez**, *Twist Bioscience*, "Integrating biomolecules and semiconductors to build a data storage system"

3:00PM **Boyan Boyanov**, *Illumina*, "DNA Sequencing for Data Storage"

Monday, May 22nd

Poster Session 6:00PM – 8:30PM

[P1] Louisa Schneider, *Silicon Storage Technology*, "Analog Tuning of Floating-Gate Cells with Sub-Elementary Charge Accuracy for In-Memory Computing Applications"

[P2] Xianzhou Shao, *IME*, "Comprehensive Study of Endurance Fatigue in the Scaled Si FeFET by in-situ Vth Measurement and Endurance Enhancement Strategy"

[P3] Noboru Shibata, *KIOXIA*, "7-Bit/2Cell (X3.5), 9-Bit/2Cell (X4.5) NAND Flash Memory: Half Bit technology"

[P4] Tobias Ziegler, *RWTH Aachen University*, "Eliminating Capacitive Sneak Paths in Associative Capacitive Networks based on Complementary Resistive Switches for In-Memory Computing"

[P5] Amir Regev, *Weebit Nano*, "Demonstration of SMT-reflow Immune and SCA-resilient PUF on 28nm RRAM device array"

[P6] Sola Woo, *Georgia Tech*, "Design of Ferroelectric-Metal Field-Effect Transistor for Multi-Level-Cell 3D NAND Flash"

[P7] Wei-Chih Chien, *Macronix*, "A Comprehensive Study on the Pillar Size of OTS-PCM Memory with an Optimized Process and Scaling Trends Down to Sub-10 nm for SCM Applications"

[P8] Viktor Markov, *Microchip*, "Effect of high-temperature bake on RTN statistics in floating gate flash memory arrays"

[P9] Z. Asher Bai, *Independent researcher*, "Dielectric Relaxation Performance of DRAM Storage Capacitors and Ways of Improvements"

[P10] Nicola Lepri, *Politecnico di Milano*, "In-memory neural network accelerator based on phase change memory (PCM) with one-selector/one-resistor (1S1R) structure operated in the subthreshold regime"

[P11] Bastien Giraud, *CEA-List*, "Benefits of Design Assist Techniques on Performances and Reliability of a RRAM Macro"

[P12] Yasuhiro Taniguchi, *Floadia*, "SONOS Embedded Flash IP Using Trap-Depth-Controlled SiN Film Enabling Data Retention more than 10 years at 200℃"

[P13] Takuto Nishimura, *The University of Tokyo*, "Stochastic Computing-based Computation-in-Memory (SC CiM) Architecture for DNNs and Hierarchical Evaluations of Non-volatile Memory Error and Defect Tolerance"

[P14] David Lehninger, *Fraunhofer IPMS*, "Ferroelectric HfO2/ZrO2 Superlattices with Improved Leakage at Bias and Temperature Stress"

Monday May 22nd, 2023

08:30AM **Thomas Mikolajick**, **Opening Remarks**

Session #1 8:30AM – 10:20AM Keynotes

Chairs: **Thomas Mikolajick**, *Namlab/TU Dresden*
Dirk Wouters, *RWTH Aachen*

8:50AM **[1.1] Alessandro Grossi**, *Infineon*, "28nm Data Memory with Embedded RRAM Technology in Automotive Microcontrollers"

9:20AM **[1.2] Jeongdong Choe**, *TechInsights*, "Recent Technology Insights on STT-MRAM: Structure, Materials, and Process Integration"

9:50AM **[1.3] Sunil Shim**, *Samsung*, "Trends and Future Challenges of 3D NAND Flash Memory"

10:20AM *Break*

Session #2 10:50AM – 12:05PM 3D NAND I

Chairs: **Antonio Arreghini**, *imec*
Haitao Liu, *Micron*

10:50AM **[2.1] Suhwan Lim,** *Samsung*, "Improvement of GIDL-assisted Erase by using Surrounded BL PAD Structure for VNAND"

11:15AM **[2.2] Soochan Kyle Chung**, *Samsung*, "Process Improvements for 7th Generation 1Tb Quad-Level Cell 3D NAND Flash Memory in Mass Production"

11:40AM **[2.3] Gianluca Nicosia**, *Micron*, "Distributed Cycling in Charge Trap-Based 3D NAND Arrays: Model and Qualification Tests Implications"

12:05PM *Lunch (Provided) / Committee Luncheon*

Session #3 2:05PM – 3:20PM 3D DRAM & Selectors

Chairs: **Thomas Mikolajick**, *Namlab/TU Dresden*
Shiva Shetty, *Infineon*

2:05PM **[3.1] Wei-Chen Chen,** *Macronix*, "A Simulation Study of Scaling Capability toward 10nm for the 3D Stackable Gate-Controlled Thyristor (GCT) DRAM Device" - ***Invited***

2:30PM **[3.2] Tao Dou**, *CXMT*, "A 3D Stackable 1T1C DRAM: Architecture, Process Integration and Circuit Simulation"

2:55PM **[3.3] Yi Jiang**, *CXMT*, "Vertical Channel Transistor (VCT) as Access Transistor for Future 4F2 DRAM Architecture" – ***Late News***

Poster Presentations 3:30PM – 4:00PM

Chair: Gill Lee, *Applied Materials*

Reception 5:30PM – 8:30PM

Sponsored by Applied Materials

Poster Session 6:00PM – 8:30PM

Chair: Gill Lee, *Applied Materials*

Tuesday May 23rd, 2023

Session #4 8:30AM – 10:10AM Ferro

Chairs: **Jun Okuno**, *SONY*
Jaewoo Kim, *CXMT*

8:30AM **[4.1] Konrad Seidel**, *Fraunhofer*, "Hafnium oxide-based Ferroelectric Memories: Are we ready for Application?" - ***Invited***

8:55AM **[4.2] Zhuo Chen**, *imec*, "Improved MW of IGZO-channel FeFET by Reading Scheme Optimization and Interfacial Engineering"

9:20AM **[4.3] Julie Laguerre**, *CEA-LETI*, "Memory Window in Si:HfO2 FeRAM arrays: Performance Improvement and Extrapolation at Advanced Nodes"

9:45AM **[4.4] Laurent Breuil**, *imec*, "Optimization of Retention in Ferroelectricity Boosted Gate Stacks for 3D NAND"

10:10AM *Break*

Session #5 10:40AM – 12:20PM 3D NAND II

Chairs: **Yong Kyu Lee**, *Samsung*
Bruce Hsu, *Macronix*

10:40AM **[5.1] Biswajit Ray**, *University of Alabama*, "Towards Improving Ionizing Radiation Tolerance of 3-D NAND Flash Memory" - ***Invited***

11:05AM **[5.2] Andrew Bicksler**, *Micron*, "Physical Model and Characteristics of 3D NAND Memory Cell Metastability Issues under High Temperature Stress"

11:30PM **[5.3] Song-hyeon Kuk**, *Korea Advanced Institute of Science and Technology*, "Proposal of P-Channel FE NAND with High Drain Current and Feasible Disturbance for Next Generation 3D NAND"

11:55PM **[5.4] Sana Rachidi**, *imec*, "Enabling 3D NAND Trench Cells for Scaled Flash Memories"

12:20PM *Lunch (Provided)*

Session #6 1:50PM – 3:30PM Systems, STT & RRAM

Chairs: **Martin Lueker-Boden**, *Western Digital*
Robert Glazewski, *Texas Instruments*

1:50PM **[6.1] Antonino Conte**, *ST Microelectronics*, "An 18nm ePCM with BJT selector NVM design for advanced microcontroller applications" - ***Invited***

2:15PM **[6.2] Kazuma Hasegawa**, *KIOXIA*, "Low Power and Thermal Throttling-less SSD with In-Package Boost Converter for 1000-WL Layer 3D Flash Memory"

2:40PM **[6.3] Bhagwati Prasad**, *Indian Institute of Science Bengaluru*, "Voltage Control of Magnetism: Low-Power Spintronics" - ***Invited***

3:05PM **[6.4] Donato Francesco Falcone**, *IBM Research Europe - Zurich*, "Physical modeling and design rules of analog Conductive Metal Oxide-HfO2 ReRAM"

3:30PM *Break*

Panel Discussion 4:00PM – 5:30PM

Topic: "Can 3D structuring be a technology driver for memory like it was for NAND?"

Moderator: **Tomoya Sanuki**, *KIOXIA*

Panellists: **Jeongdong Choe**, *TechInsights*
Alessandro Grossi, *Infineon*
Jin-Woo Han, *Samsung*
Sony Varghese, *Applied Materials*
Subhali Subhechha, *imec*

Banquet 7:00PM – 9:00PM

Wednesday May 24th, 2023

Session #7 8:30AM – 10:10AM Neuromorphic/In-Mem

Chairs: **Sangbum Kim**, *Seoul Nat. Univ.*
Nhan Do, *Microchip*

8:30AM **[7.1] Sebastien Couet**, *imec*, "Spin-orbit torque MRAM for ultrafast cache and neuromorphic computing applications" - ***Invited***

8:55AM **[7.2] Po Hao Tseng**, *Macronix*, "SLC and MLC In-Memory-Approximate-Search Solutions in Commercial 48-layer and 96-layer 3D-NAND Flash Memories"

9:20AM **[7.3] Franz Müller**, *Fraunhofer IPMS*, "Multi-Level Operation of ferroelectric FET Memory Arrays for Compute-In-Memory Applications"

9:45AM **[7.4] Subhali Subhechha**, *imec*, "Demonstration of multilevel multiply accumulate operations for AiMC using engineered a-IGZO transistors-based 2T1C gain cell arrays"

10:10AM *Break*

Session #8 10:40AM – 11:50AM 3D Processing

Chairs: **Andrea Redaelli**, *ST Microelectronics*
Dirk Wouters, *RWTH Aachen*

10:40AM **[8.1] Bala Haran**, *Applied Materials*, "Materials Enabled Memory Scaling and New Architectures" - ***Invited***

11:05AM **[8.2] Pradeep Subrahmanyan**, *Applied Materials*, "Overlay Control in HAR device integration"

11:30AM **Thomas Mikolajick**, **Closing Remarks**

11:40AM **Antonio Arreghini**, **Best Paper Award Announcement**